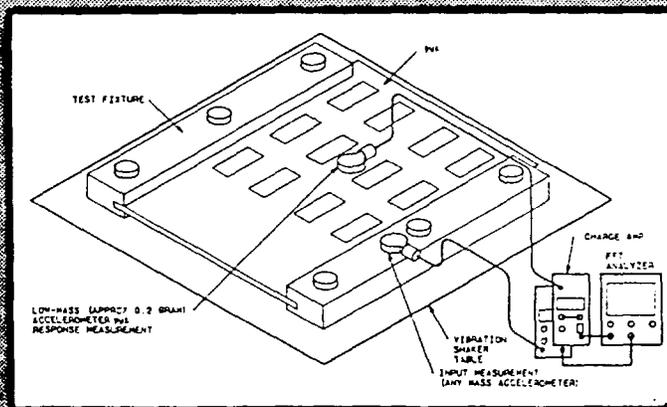
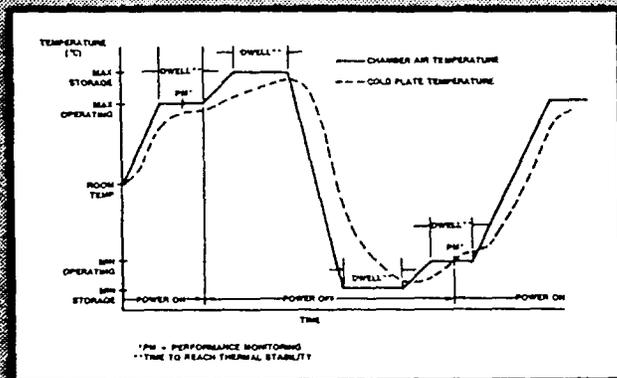
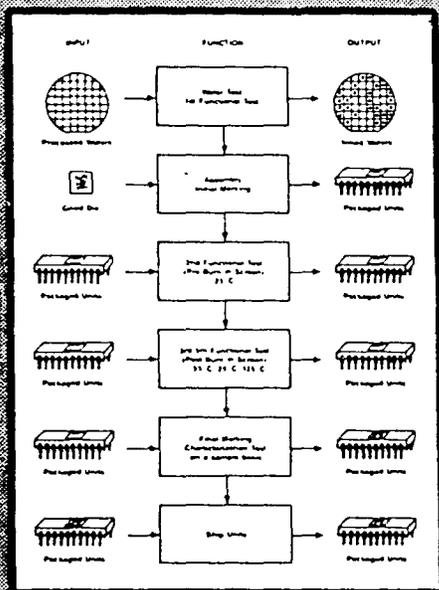


ENVIRONMENTAL STRESS SCREENING REQUIREMENTS AND APPLICATION MANUAL FOR NAVY ELECTRONIC EQUIPMENT



**ENVIRONMENTAL STRESS SCREENING
REQUIREMENTS
AND
APPLICATION MANUAL
FOR
NAVY ELECTRONIC EQUIPMENT**



APPROVED:



DEPUTY CHIEF ENGINEER FOR
DESIGN AND MANUFACTURING QUALITY
NAVAL SEA SYSTEMS COMMAND

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PREFACE



Environmental stress screening (ESS) is a process that has gained wide acceptance as an effective means of discovering defective parts and material. Effective application of ESS reduces in-plant rework costs by disclosing defects due to parts, workmanship, and manufacturing process deficiencies. ESS also decreases maintenance and support costs attributable to early life failures of fielded systems and improves availability during initial deployment. A closed loop corrective action process, dedicated to determining defect cause and instituting corrective action to prevent recurrence, must be an integral part of ESS to assure maximum benefit.

In order to affect continuous process improvement, program managers must tailor the information in this document for the development of solicitation requirements and must allow the contractor implemented processes to change when warranted and justified by the facts so that the processes will be adaptable to changing circumstances.

The efficacy of a process is dependent upon the degree of understanding of all involved of the elements and purpose of the process. This guide is issued to provide the means for this understanding.

A handwritten signature in dark ink, appearing to read "D. M. Altwegg".

D. M. ALTWEGG

Deputy Chief Engineer for Design
and Manufacturing Quality

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SECTION 1

INTRODUCTION

1.1 SCOPE

The scope and purpose of this document is to define requirements for NAVSEASYSCOM, its equipment and spares contractors, and Class A and B depots for conducting Environmental Stress Screening (ESS) during Full Scale Development (FSD), production and reprocurments, spares and repair on Weapons and Combat Systems. It is intended for use by Navy Program Managers as the baseline minimum ESS requirements for contract Statements of Work (SOW), and by design and manufacturing engineers and depot repair facilities for implementation. The requirements presented herein represent fundamental requirements at the part level, Printed Wiring Assembly (PWA), and higher indenture levels.

NAVSEA procuring, spares, and repair activities must address those aspects of ESS which are associated with specifying ESS requirements, and must be involved with the equipment, spares, and part manufacturer to ensure the requirements are being met. Equally important in the ESS process is the selection of an equipment/spares contractor or Class A/B depot willing and capable of implementing the requirements in this manual. A fundamental criteria in FSD, production, spares and repair facilities selection must be the user's stated, perceived, and demonstrated ability to comply with these minimum requirements.

The concept that ESS is simple or should be developed by the equipment contractor or spares/repair facility leads to insufficient SOW requirements during contract preparation, insufficient corporate funding, and buy-in by inexperienced and otherwise unqualified companies, and inadequate planning/budgeting by the repair facilities. Equipment specifications, program budgets, contractor bids, program and manufacturing/repair plans which fail to impose the requirements of Section 2 herein must be considered suspect with regard to providing "quality products to the Fleet." It is incumbent on NAVSEA, our equipment contractors, and our repair facilities to understand, plan, design, and implement these ESS requirements to ensure that Fleet readiness is not compromised by part and/or workmanship defects. Contractors and repair facilities are responsible for using sound engineering principles to develop an ESS plan. Once this is complete, deviations from the standard will be considered.

This manual provides both ESS requirements and application information concerning the implementation of ESS. Part screening, upgrade screening, and part rescreening are all considered part of ESS. The requirements for these screens are contained in Section 2 and must be reflected in all contract SOW requirements. Section 3 provides detailed information on the application of ESS at the part level along with tailoring considerations. Section 4

contains application information for Thermal Cycling Stress Screening (TCSS), and Section 5 the same for Random Vibration Stress Screening (RVSS).

The remainder of this section focuses on how to utilize this manual and provides some basic definitions that are applied consistently throughout to establish a baseline of terminology.

1.2 APPLICATION OF THIS ESS MANUAL

The ESS requirements contained in Section 2 must be invoked in all contracts which contain mission essential Weapons and Combat Systems electronic hardware. This may exclude shore test equipment and feasibility models that will not be delivered to the fleet. All ESS requirements must be accomplished at the lowest feasible level of assembly in accordance with Figure 1-1. Per this figure, all electrical/electronic parts shall be purchased as screened parts to the minimum quality levels of Section 2.2.1 during FSD production/reprocurement/spares/repair. All other active parts shall be upgrade screened per Table 2-1 (for Integrated Circuits) and Table 2-2 (for Discrete Semiconductors). All parts meeting the minimum quality levels of Section 2.2.1 and all upgrade screened parts shall be subjected to additional part requirements in accordance with Section 2.2.2.

In addition to part level screening/additional part requirements, all contracts for equipment in FSD, or production for equipment that will complete FSD after the date of this manual shall require, as a minimum, two levels of TCSS and one level of RVSS in accordance with Section 2.3.1, Section 2.3.2, paragraphs 1 or 2, and Section 2.4.1, respectively. TCSS and RVSS may be performed together.

In addition to part level screening/additional part requirements, all production contracts for equipment completing FSD prior to the date of this manual, or a reprocurement, or a contract for spares, or a Class A/B repair depot, shall require one level of TCSS and one level of RVSS, as a minimum, in accordance with Section 2.3.2, paragraph 3, and Section 2.4.1, respectively. However, a TCSS, RVSS, TCSS combination screen, as discussed above, is preferred and should be implemented whenever possible.

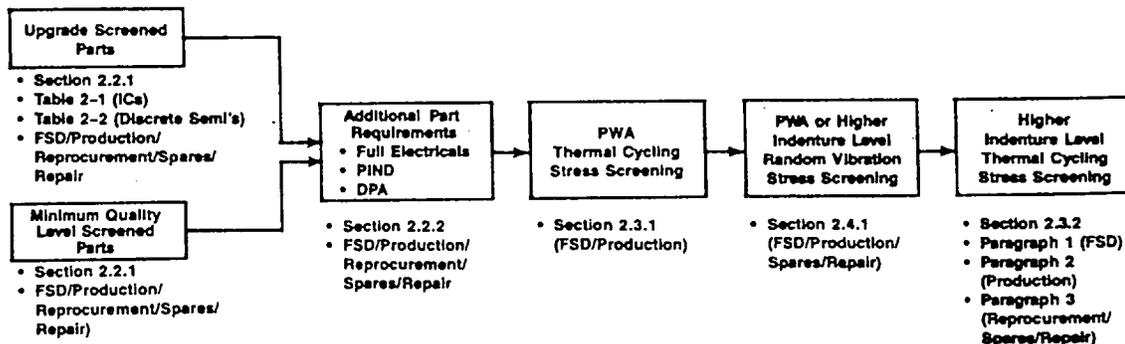


Figure 1-1. ESS Flow Diagram

The remaining sections (Section 3 - Parts, Section 4 - TCSS, and Section 5 - RVSS) provide application information, considerations for special cases, and tailoring aspects of the ESS requirements presented in Section 2.

1.3 DEFINITIONS

As is the case with almost any technical discipline, the degree to which it is understood, or misunderstood, significantly affects its proper utility. This potential problem area becomes real when technical requirements are being addressed. While the subsequent definitions are not universal, they are provided so that users of this manual will be reading, interpreting, and applying the same baseline terms.

BONDED STOCK - Terminology used for ensuring part integrity. Bonded stock occurs after the part manufacturer has placed the parts in a sealed container. The container must protect the devices from handling as well as ESD damage. If the parts are repackaged or lots split outside the manufacturers facility, the parts are no longer considered to be in bonded stock.

COLD PLATE - This terminology is used in thermal cycle stress screening. The original definition of a cold plate refers to a housing that would circulate cold fluid to assist in cooling the thermal chamber. For the purposes of this document, the cold plate refers to a true cold plate or a portion of the fixture that holds the hardware.

DESTRUCTIVE PHYSICAL ANALYSIS (DPA) - Systematic, logical, detailed examination during various states of physical disassembly of a part to identify problems or discrepancies and their probable cause. Normally conducted to verify conformance with applicable design and process requirements.

EQUIPMENT OPERATING DESIGN SPECIFICATION LIMITS (Thermal) - Maximum and minimum operating temperature limits to which an equipment is designed to withstand that are imposed by the equipment specification or contract.

EQUIPMENT STORAGE SPECIFICATION LIMITS (Thermal) - Maximum and minimum storage temperature requirements that are imposed on a design by the equipment specification or contract.

GLASSIVATION (not to be confused with the term passivation) - The top layer of transparent insulating material that covers the active chip area including metallization except bonding pads and beam leads, and provides protection of the junctions and surfaces of semiconductor chips from harmful elements and particles.

INPUT STIMULUS - The vibration level measured on a fixed edge of the Printed Wiring Board or mounting fixture undergoing screening.

LATENT DEFECT - A flaw in a part or item that would eventually prevent it from meeting its functional requirement when operating within its specified environment and within its specified lifetime.

MANUFACTURING DEFECT - A flaw caused by in-process errors or uncontrolled conditions during assembly, test, inspection, or handling.

MINIMUM QUALITY LEVEL SCREENED PARTS - Parts which have been subjected to a process or combination of processes on a 100% basis for the purpose of identifying and eliminating defective, abnormal, or marginal parts. Each part must be, as a minimum, in full compliance with MIL-STD-883 Method 5004, for integrated circuit devices; MIL-S-19500 Table 11, for semiconductor devices; and applicable test methods of MIL-STD-202 for Established Reliability (ER) devices. (See applicable Military Specification for specific devices for test methods).

MODULE - A self-contained collection of chassis mounted parts and/or PWAs within one package performing a specific function or group of functions and is removable as a single package from an operating system.

NEW TECHNOLOGY PART - A semiconductor device, integrated circuit, or hybrid circuit that is available for sale by a part manufacturer, but which has been on the market for less than two years.

NORMAL INCOMING TESTING - Incoming process checks and/or tests on parts, performed by the equipment contractor, spares contractor, or Class A or B depot, that are part of their existing incoming processes, and which form the basis of part acceptance from the part manufacturer or vendor.

PART - In most cases a nonrepairable, throwaway, electrical/electronic item (e. g., integrated circuit, resistor, capacitor, diode, transistor, transformer, hybrid, etc.). Some hybrids are repairable.

PART FAMILY - This term is used in calculating part history and failure rates. A part family is defined as a group of parts that are manufactured on the same production line which may have different functions but utilize the same manufacturing techniques and same part technology, i.e. VLSI 1 micron parts cannot be grouped with VLSI .8 micron parts.

PARTICLE IMPACT NOISE DETECTION (PIND) TEST - An amplified acoustical test using electromechanical methods for detecting loose particles in the cavity of an electronic device.

PASSIVATION - The growth of an oxide layer on the surface of a semiconductor to provide electrical stability by isolating the transistor surface from electrical and chemical conditions (not to be confused with glassivation).

PERFORMANCE MONITORING - This terminology is used during the temperature cycling and refers to the powered on functional monitoring of the equipment being screened. Performance monitoring should be limited in length, but still exercise as much of the hardware as possible. When performance monitoring complex systems, a complete functional test may not be a feasible alternative due to the testing time required to fully performance monitor the entire system. If a system test takes a long time, generally over 10 minutes, the screening effectiveness will be reduced and the cost to perform the screen will be driven up. If feasible, alternatives to long testing may be used. These include switching parameters tested each cycle until the unit has exercised all feasible functional operations and a scaled back testing sequence.

PRINTED WIRING ASSEMBLY (PWA) - A single printed wiring board containing a group of interconnected parts which are mounted thereon. Equivalent terminology is circuit card assembly and printed circuit assembly.

PRINTED WIRING BOARD (PWB) - An unpopulated printed wiring assembly (bare board), Equivalent terminology is circuit card and printed circuit card.

PRODUCTION LOT - A production lot consists of devices manufactured on the same production line(s) by means of the same production technique, materials, controls, and design.

PRODUCTION LOT DATE CODE - A three or four digit number which identifies the six-week period of time in which an inspection lot was sealed. The first two digits identify the year (only one if single year). The last two digits identify the week.

RANDOM VIBRATION STRESS SCREEN - Manufacturing process using vibration excitation where magnitude and frequency are specified by a probability distribution function.

REPROCUREMENT - An older electronic system that has not been designed during Full Scale Development and/or during any of its previous production procurements to conform with the ESS requirements in this manual.

SPECIFICATION CONTROL DRAWING - A detailed description of the materials, dimensions, and workmanship for something to be built, installed, or manufactured. The SCD should contain upgrade screening requirement when applicable.

STANDARD MILITARY DRAWING (SMD) - An acquisition document developed

under the SMD Program which controls the parameters and screens of microcircuit devices not available to the requirements of MIL-M-38510.

SYSTEM - A group of units interconnected or assembled to perform an overall electronic function.

THERMAL CYCLING STRESS SCREEN - Manufacturing process using thermal excursions, to expose or surface defects, where a part, PWA, module, unit, or system is repeatedly driven from a high to low and low to high temperature limits. The transition between temperature limits is defined in terms of the temperature rate of change which is expressed in degrees per minute.

UNIT - A group of modules interconnected or assembled to perform a subfunction within a system.

UPGRADE SCREENED PARTS - Parts which do not meet the minimum quality levels defined in Section 2.2.1, but have been subjected to the screening process described in Table 2-1 or Table 2-2.

SECTION 2

ENVIRONMENTAL STRESS SCREENING REQUIREMENTS

2.1 ESS PROGRAM REQUIREMENTS

The equipment contractor, spares contractor, Class A and B repair depots shall develop and implement a program for stress screening electronic hardware. The objective of this program is to expose electronic hardware to electrical and Environmental Stress Screening (ESS) at the part and one or more levels of assembly. The program shall include screening plans and procedures at the part level (vendor and incoming inspection) as well as Printed Wiring Assembly (PWA) and higher indenture levels. It is preferred that an ESS plan be developed, and may be part of the Reliability Program Plan during Full Scale Development (FSD), the Manufacturing Plan during equipment or spares production, or a plan of action and milestones during depot repair. The types and manner of application and level of severity of each stress screen are defined as a requirement herein.

The requirements specified in this document shall be followed and the screening levels proofed. It is not the intent of this document to force specific techniques on contractors but to give guidance on how these requirements can be met. If the contractor chooses to use screening techniques other than those described here-in, they shall be allowed provided enough engineering analysis has been performed to proof-out the techniques. The environmental stress screens required should be proofed on the specific hardware to ensure that the required environments are sufficient to precipitate defects, and stress levels will not cause equipment degradation due to overstress. Any variation or deviation from these requirements shall be approved by NAVSEA prior to implementation, and will only be considered providing engineering data justifying the change is furnished along with the request.

THE REQUIREMENTS OF THIS DOCUMENT DO NOT RELIEVE THE
USER FROM PERFORMING SOUND ENGINEERING ANALYSES.

2.2 PART LEVEL SCREENING REQUIREMENTS

2.2.1 UPGRADE SCREENING REQUIREMENTS

Minimum part quality level requirements along with the upgrade screening requirements are as follows:

Table 2-1

100% Upgrade Screening Requirements for Microcircuits

SCREEN*	METHOD 5004 MIL-STD-883	REMARKS
Stabilization Bake	1008 Condition C	Required**
Temperature Cycling	1010 Condition C	Required, no waivers.
Constant Acceleration	2001, Condition E, Y1	Optional
Burn-In Test	1015, 160 Hours at 125°C	FSD - Steady State or Dynamic required, no waivers. Production - Steady State or Dynamic for large quantities.***
Final Electrical Tests		
- Static Test	5005, Max Temp 5005, Min Temp	Required, no waivers. Required, no waivers.
- Dynamic (or Functional) Test	5005, Max Temp 5005, Min Temp	Required**** Required****
- Switching Tests	5005, 25°C	Required, no waiver
Hermetic Seal		
- Fine	1014, Condition A or B	Required, no w?
- Gross	1014, Condition C,D,E or F	Required, no w

- * The upgrade screening sequence shall be in the same sequence table unless approved by NAVSEA prior to implementation.
- ** May be waived if performed by part manufacturer and docume available.
- *** May be waived in special cases for small quantities.
- **** May be waived in special cases for very high speed parts.

Table 2-2

100% Upgrade Screening Requirements for Discrete Semiconductors

SCREEN*	TABLE II MIL-S-19500 MIL-STD-750	CONDITION	REMARKS
High Temperature Storage	1032	24 Hours, max. storage temp.	Required **
Thermal Shock	1051	20 cycles	Required, no waivers.
-Glass Body Diodes	1056	10 cycles	
Surge	4066	B	Required, no waivers.
Thermal Response		As Specified	
-Transistors			
--Power FET's	3161		Required, no waivers.
--Bipolar	3131		Required, no waivers.
-Diodes	3101		Required, no waivers.
-IGBT	3103		Required, no waivers.
-GaAs	3104		Required, no waivers.
Constant Acceleration	2006	Y1 Direction 20,000 Gs 48 Hours (150°C)	Optional
High Temperature Reverse Bias			
-Transistors	1039	A	Required, no waivers.
-Diodes, Rectifiers	1038	A	Required, no waivers.
-Power FET's	1042	B	Required, no waivers.
Power Burn-In			
-Transistors	1039	B, 160 Hours	Required, no waivers.
-Diodes	1038	B, 96 Hours	Required, no waivers.
-Thyristors	1040	-, 96 Hours	Required, no waivers.
-Power FET's	1042	A/C, 160 Hours	Required, no waivers.
Final Electrical Tests		Group A	
-Static Tests		Sub.2, 25°C	Required, no waivers.
Hermetic Seal		G or H	
-Fine	1071	A, C, D, E, J or K	Required, no waivers.
-Gross	1071		Required, no waivers.

* The upgrade screening sequence shall be in the same sequence as this table unless approved by NAVSEA prior to implementation.

** May be waived if performed by part manufacturer and documentation is available.

Microcircuits

Microcircuits shall be MIL-M-38510 Class B as a minimum, or procured to full compliance with MIL-STD-883 Method 5004. All other microcircuits shall be upgrade screened on a 100% basis to the requirements as detailed in Table 2-1.

Discrete Semiconductors

Discrete semiconductors shall be MIL-S-19500 Level JANTX as a minimum. All other discrete semiconductors shall be upgrade screened on a 100% basis to the requirements as detailed in Table 2-2.

Passive Parts

Passive parts shall be selected from Established Reliability (ER) military specifications and shall meet, as a minimum, the ER failure rate level of R or better (i.e. S), except for solid tantalum capacitors (MIL-C-39003F) which shall be ER failure rate level of B (Weibull) or better (i.e., C or D). When these parts do not exist, the contractor shall use an ER level less than R or other military parts as allowed by contract.

Upgrade Screening Documentation

Upgrade screening may be performed by the part manufacturer, an independent testing laboratory, the equipment contractor, the spares contractor, or the depot. Any screens performed by the part manufacturer do not need to be repeated during upgrade screening. If performed by the part manufacturer, certification of test and results must be provided by the part supplier. If performed by an independent test laboratory, the equipment contractor, the spares contractor, or the depot, upgrade screening results shall be available for review.

2.2.2 ADDITIONAL PART REQUIREMENTS (PART RESCREENING)

Additional part level requirements, also know as part rescreening, shall be imposed on the equipment contractor, spares contractor, or depot facility to prevent introduction of defective electronic parts in the manufacturing process. The part rescreening requirements may be reduced or deleted with technical justification (See section 3.5.1).

Exclusion of Electrical Testing for Upgrade Screened Parts

If upgrade screened parts have been electrically tested by the equipment contractor, an independent test facility, or spare/repair depot, it is unnecessary to repeat any of the additional electrical test requirements on these parts. Electrical tests required for upgrade screening may be combined with the electrical test requirements of this Section.

Microcircuits

All microcircuits procured shall be subjected to the following additional part requirements prior to installation into higher assemblies:

1. Electrical Tests

- All devices shall be subject to electrical Go/No-Go static, dynamic or functional, and switching tests at -55°C and +125°C. If parts are not procured as MIL-STD parts, the electrical tests must be performed at the parts operating maximum and minimum operating temperatures.
- Reduce to sample testing or delete per Section 3.5.1 (Consideration for Reduced Electrical Performance Testing), if approved by NAVSEA.
- For very high speed microcircuits, selected ac parameters may be excluded if these parameters are beyond the capability of the test equipment. Any exclusion shall be approved by NAVSEA prior to implementation.

2. Particle Impact Noise Detection Testing (PIND)

- Required on all hybrids and all unglassivated cavity devices, if not previously performed. If parts can be proven to be glassivated, PIND need not be performed.
- Use of getter material in hybrids shall be approved by NAVSEA.
- Expand to include Conductive Particle Detection Test on hybrids per Section 3.5.2, if warranted.

3. Destructive Physical Analysis (DPA)

- Minimum 2 parts per production lot date code. If a full pre-cap visual inspection is performed in accordance with the guidelines of MIL-STD-883 Method 2010, Condition A, DPA may be waived with Procuring Activity approval.
- Expand to include Residual Gas Analysis, and/or Surface Impurity Analysis per Section 3.5.3, if warranted.
- Waive requirement per Section 3.5.3, if approved by NAVSEA.
- Upgrade screened and/or new technology parts may not be waived, unless technical justification is provided and approved by NAVSEA.

-
- Perform DPA sequence as shown in Table 2-3.

Discrete Semiconductors

All semiconductors shall be subjected to the following prior to installation into higher assemblies:

1. Electrical Tests

- All devices shall be subject to electrical Go/No-Go static tests at their maximum and minimum operating temperature limits.
- Reduce to sample testing per Section 3.5.1, if approved by NAVSEA.

2. Particle Impact Noise Detection Testing

- Required on all unglassivated cavity semiconductor devices.
- Not required if performed by part manufacturer

3. Destructive Physical Analysis

- Minimum 2 parts per lot date code.
- Expand to include Residual Gas Analysis, and/or Surface Impurity Analysis per Section 3.5.3, if warranted.
- Waive requirement per Section 3.5.3, if approved by NAVSEA.
- Upgrade screened and/or new technology parts may not be waived.
- Perform DPA sequence as shown in Table 2-3 (where applicable). Tests that are designated as Special Tests need only be performed when additional testing is necessary.

Passive Parts

Discrete passive parts procured shall be subjected to a contractor's or Class A/B depot's normal incoming inspection. Additional part level requirements for problem part types should be added per Section 3.5.3, if warranted.

Table 2-3. Required Semiconductor DPA Sequence Flow

Inspection Test	Purpose
External Visual	Proper marking, workmanship, no evidence of damage.
Hermeticity	Leak test (fine/gross) to determine potential seal damage.
Residual Gas Analysis (Special Test)*	Mass spectrometer system with special chambers and fixtures for detecting very small quantities of internal water vapor or gas contamination.
Internal Visual	Semiconductor die inspection, wire bonding, internal package construction.
Configuration	Photograph of die and package to check for conformance to design documentation, and thus configuration changes.
Bond Pull	Good lead attachment to semiconductor die and package.
Scanning Electron Microscope (SEM) Inspection	Good Aluminum interconnect coverage and condition. Adequate oxide step coverage.
Die Shear	Good semiconductor die attachment to package.
Surface Impurity Analysis (Special Test)*	Scanning electronic spectroscopy to detect trace surface impurities.
Test Report	Maintain records for possible future problems and/or comparison for future procurements.

* Special Test need only be performed if warranted

2.3 THERMAL CYCLING STRESS SCREENING (TCSS) REQUIREMENTS

All Combat and Weapon Systems in the FSD phase or entering first production after July 1988 shall receive two levels of TCSS, one per Section 2.3.1 and one per Section 2.3.2. Random Vibration Stress Screening (RVSS) per Section 2.4 shall be completed either

between the two TCSS levels or in combination with one of the TCSS levels. When TCSS and RVSS are combined, RVSS shall be required towards the end of TCSS if combined at the PWA indenture level, or towards the beginning of TCSS if combined at a higher indenture level.

2.3.1 PRINTED WIRING ASSEMBLY (PWA) LEVEL THERMAL CYCLING REQUIREMENTS

PWA TCSS requirements are summarized below. All temperature parameters are hardware response.

1. Number of Thermal Cycles:

- 20 cycles minimum if Temperature Rate of Change $\geq 15^{\circ}\text{C}/\text{minute}$ (Upper Limit $20^{\circ}\text{C}/\text{minute}$)
- 25 cycles minimum if Temperature Rate of Change ≥ 10 but $< 15^{\circ}\text{C}/\text{minute}$
- 30 cycles minimum if Temperature Rate of Change ≥ 5 but $< 10^{\circ}\text{C}/\text{minute}$
- $5^{\circ}\text{C}/\text{minute}$ shall be the lower limit.

2. Temperature Range:

- $\Delta T \geq 120^{\circ}\text{C}$, as a hardware response from minimum to maximum temperature limits.
- If unattainable, increase number of Thermal Cycles by 5 for each 10°C drop in ΔT below 120°C .
- Minimum ΔT shall be 70°C .

3. Temperature Rate of Change:

- Temperature rate of change = $\Delta T/t$

where: ΔT = Temperature Range (See 2 above), t = time in minutes required for the electronic part with the largest thermal mass (excluding magnetics and connectors) or nonmetallic portion of the PWB surface to traverse ΔT and reach thermal stability (See Figure 2-1). The temperature rate of change, for calculation purposes, can be taken from the increasing or decreasing portion of the cycle. The thermocouple used to verify the response shall be insulated from the chamber air.

-
- All power to the PWA shall be removed when temperature rate of change is measured.
 - Controlled chamber air overshooting/undershooting to achieve a higher temperature rate of change is permissible provided parts and materials are not thermally overstressed.
4. Thermal Stability:
- Thermal Stability is considered to have occurred when the electronic part with the largest thermal mass (excluding magnetics and connectors) or non-metallic portion of the PWB surface is within 5°C of the Temperature Range Limits.
 - Measurement shall be by a thermocouple mounted directly on the electronic part or PWB surface. The thermocouple shall be insulated from the chamber air.
5. Dwell Time at Temperature Range Limits:
- Dwell Time at the upper and lower Temperature Range Limits need only be long enough to reach Thermal Stability (as defined above).
6. Failure Free Temperature Cycle:
- A functional test shall be performed after the PWA level TCSS. If a PWA RVSS is to be performed, the functional test may be delayed until after the RVSS.
 - Failed PWAs shall be repaired/reworked.
 - Repaired/Reworked PWAs, if not subjected to subsequent TCSS at a higher indenture level, shall be subjected to an additional temperature cycle followed by a functional test. Failed PWAs shall repeat this sequence no more than two times. In the event that a PWA fails the second failure free cycle for the same reason as the first failure free cycle, recommended corrective actions/alternative approaches shall be provided to NAVSEA. Application aspects are discussed in Section 4.5.
 - Repaired/Reworked PWAs, when subjected to subsequent TCSS at a higher indenture level, shall be reintroduced into the production flow process without requiring a failure free cycle.
7. Performance Monitoring:
- Not required.
-

8. Power On/Off Cycle:

- Input power or power on/off cycling not required.

2.3.2 HIGHER INDENTURE LEVEL THERMAL CYCLING REQUIREMENTS

1. Full Scale Development (FSD):

- Must be preceded by PWA level (TCSS) per Section 2.3.1 and Random Vibration Stress Screening (RVSS) per Section 2.4. TCSS and RVSS may be combined per Section 2.3.
- Number of thermal cycles: 20 cycles minimum. May be reduced if data justifies and approved by NAVSEA. See Section 4.4.
- Minimum Temperature Range (ΔT): Equipment storage specification temperature limits (minimum to maximum).
- Temperature Rate of Change: $\geq 5^{\circ}\text{C}/\text{minute}$ measured by a thermocouple attached to the cold plate or non-metallic portion of the largest Printed Wiring Board (PWB) if no cold plate exists. The thermocouple shall be insulated from the chamber air.
- Failure Free Period: Last cycle shall be failure free.
- Performance Monitoring: Required on each increasing portion of the cycle at equipment operating design specification temperature limits (maximum and minimum).
- Power On/Off Cycling: Power on is required each cycle during only the positive increasing portion of the thermal cycle within the equipment operating design specification limits (maximum and minimum). Power shall be off during the remainder of the thermal cycle.
- Thermal Stability/Dwell Times: Defined in PWA Thermal Cycling Requirements.

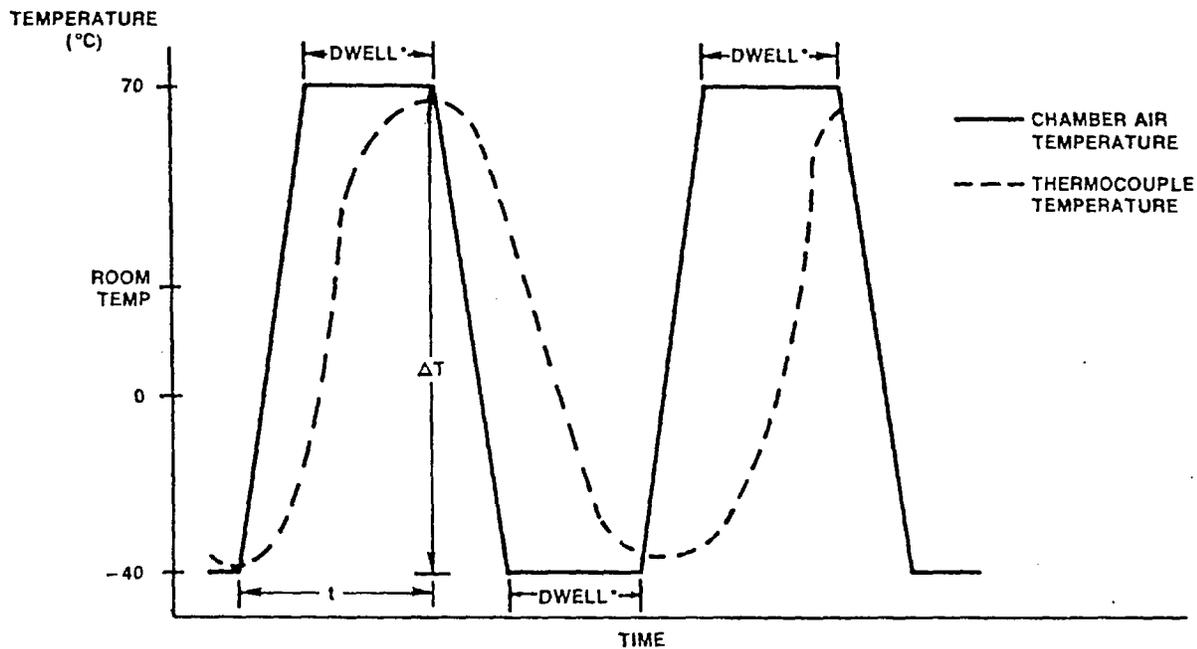
2. Production (When Preceded by PWA Thermal Cycling):

- Same as 1 above, except as noted below.
- Performance Monitoring: Not required if test equipment not developed during FSD.

- Power On/Off Cycling: Not required if test equipment not developed during FSD.

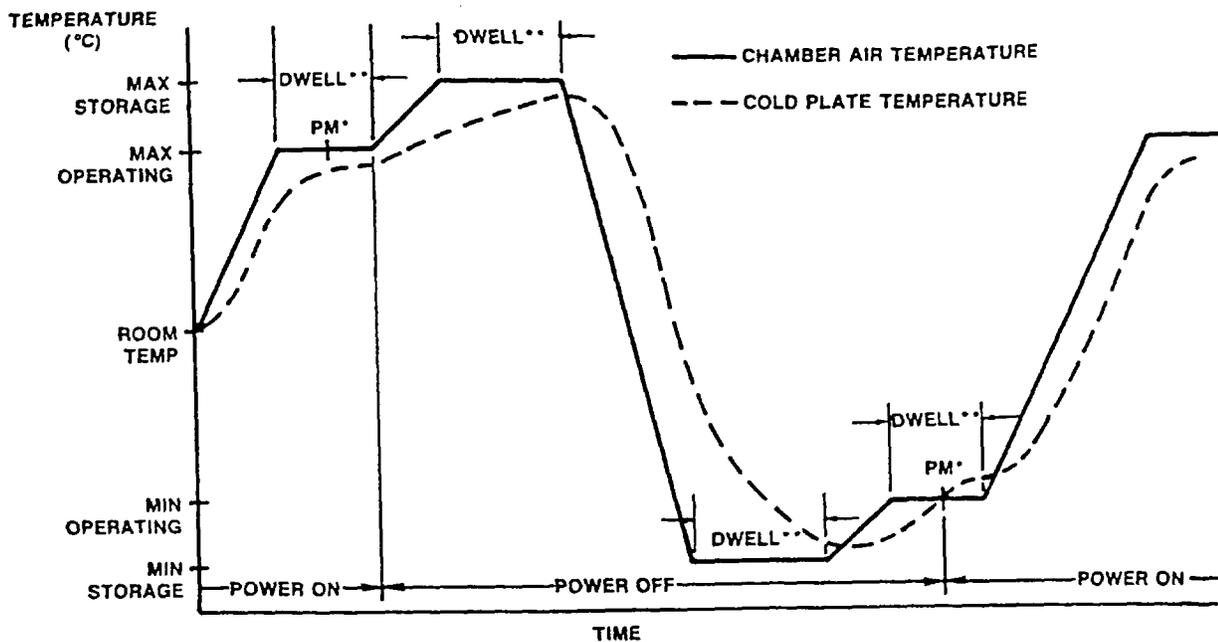
3. Reprocurement/Spares/Repair (When Not Preceded by PWA Thermal Cycling):

- Must be approved by NAVSEA prior to the start of hardware manufacturing.
- Number of Thermal Cycles: Same as PWA Thermal Cycling Requirements.
- Minimum Temperature Range (ΔT): Equipment storage specification temperature limits (minimum to maximum).
- Temperature Rate of Change: Same as PWA Thermal Cycling Requirements.
- Thermal Stability: Same as PWA Thermal Cycling Requirements.
- Dwell Time: Same as PWA Thermal Cycling Requirements.
- Failure Free Period: Last cycle shall be failure free.
- Performance Monitoring: Not required if test equipment not developed.
- Power On/Off Cycling: Not required if test equipment not developed.



*TIME TO REACH THERMAL STABILITY.

Figure 2-1. Example PWA Thermal Cycling Profile



*PM = PERFORMANCE MONITORING
 **TIME TO REACH THERMAL STABILITY

Figure 2-2. Example Higher Indenture Level Thermal Cycling Profile

2.3.3 THERMAL CYCLING PROFILE

In order to conduct the ESS thermal cycling stress screen as effectively as possible, it is necessary to obtain an effective thermal cycling profile. It is the number of thermally induced stress reversals (minimization of soaks), the temperature extremes, and the thermal rate of change of the hardware which are the principal parameters associated with disclosure of thermally sensitive manufacturing defects. The thermal performance of the chamber air is irrelevant. Thermal profiles shall be developed when performing TCSS. The profile illustrated in Figure 2-1 has been developed as a PWA TCSS example. The dwell times at temperature range limits should be minimal, as the mass of the parts is normally small with little thermal capacitance. Typical higher indenture level thermal cycling is illustrated in Figure 2-2. Higher indenture level thermal cycling may require longer dwell times to assure that the cold plate (or largest PWB) reaches the maximum and minimum temperature limits. Chamber air temperature overshooting/undershooting is an acceptable method of increasing the temperature rate of change when following the procedures delineated in Section 4.3. The equipment shall be thermally surveyed to determine the response to the stimulus. Once the response is known for the worst case thermal load and chamber conditions, the thermal chamber can be controlled or monitored at the most convenient location. Survey data relating the control point to the response shall be maintained for review.

2.4 RANDOM VIBRATION STRESS SCREENING (RVSS) REQUIREMENTS

2.4.1 RVSS REQUIREMENTS

1. Acceleration Response Spectrum:

- RVSS may be performed at any indenture level, provided an effective input stimulus (as defined in section 1) to the PWAs is achieved.
- The acceleration spectrum shall be calculated to determine the maximum allowable Power Spectral Density (PSD) level for each unique PWA regardless of the indenture level for applying RVSS.
- The values calculated shall be proof tested on actual hardware to determine if the input stimulus to the PWA is at or below a level that would result in equipment degradation. Proof testing should not damage good hardware.
- If the calculated maximum allowable PSD level is below the starting PSD profile, as shown in Figure 2-3, a corrective action plan shall be submitted for approval by NAVSEA before the start of the ESS program. As a minimum, this plan shall address proposed means to increase RVSS input (e.g. removal of heavy parts prior to RVSS or the use of a bonding agent, etc.), and RVSS effectiveness if corrective action is not implemented.
- The acceleration spectrum applied at the module and/or higher levels of indenture shall not be below Figure 2-3 due to a minority of PWA's whose design is limiting the input. Removal of these minority PWAs resulting in increased module or higher indenture level screening effectiveness is suggested. In this case, minority PWAs would be screened separately at their limiting vibration screening levels.
- Combining PWAs of similar PSD levels together to optimize effectiveness is allowable.

2. Input Stimulus:

- As a starting point, a power spectral density of .04 g^2/HZ from 20 to 2000 Hz with a 3 db/Octave roll-off from 350 to 2000 Hz shall be used as a reference. This is demonstrated in Figure 2-3(a). A roll-off of 3 db/Octave between 80 and 20 Hz may also be used if the screening facility or the equipment to be screened is not tolerant of low frequency vibration stimulus. This is demonstrated in Figure 2-3(b).

- The input stimulus shall be either random or quasi-random. If quasi-random stimulus is used, a ± 10 db tolerance shall be maintained. Other random stimuli shall maintain a ± 3 db tolerance. (See Figure 2-3).
- Notching the frequencies where maximum PWA deflection occurs (resonances), or reducing the PSD level to avoid overstressing is permissible. Reducing the PSD levels or notching more than 50 Hz requires approval by NAVSEA. If notching is employed, an accumulated band of 50 Hz max may be notched over the entire frequency spectrum unless otherwise approved by the Procuring Activity.
- It is not necessary for the RVSS input to exceed $.04 \text{ g}^2/\text{HZ}$. Input stimulus shall be measured as close as possible to the PWB edge, either on the PWB or on the fixture.

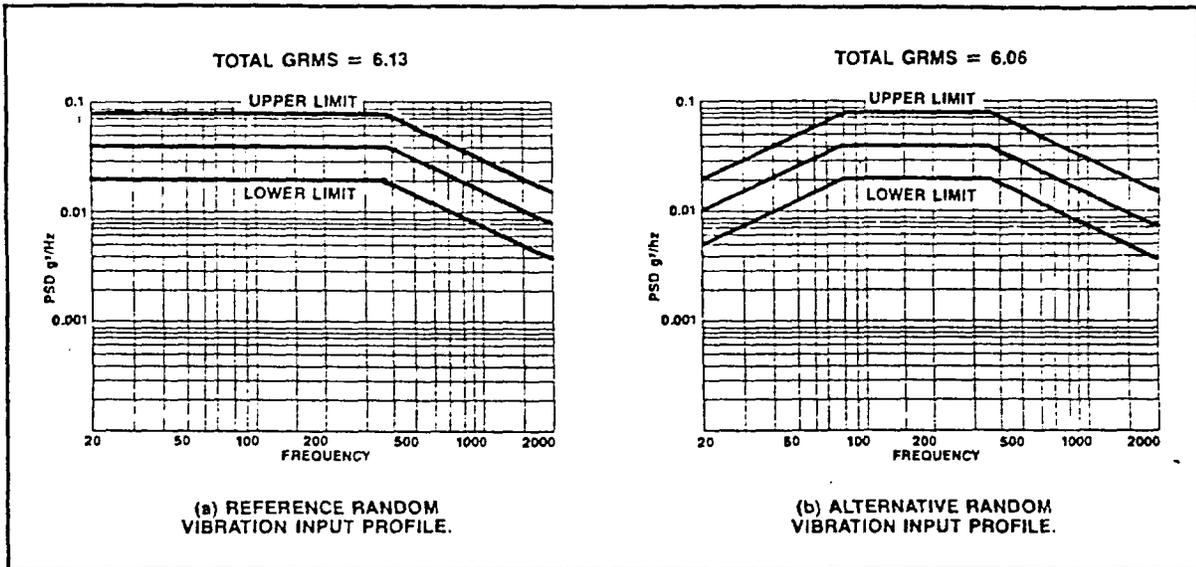


Figure 2-3. RVSS Input Profiles

3. Indenture Level:

- RVSS may be applied in one axis at one indenture level and another axis at a higher indenture level.
- Fixtures (including equipment drawers, PWB racks, cabinets, etc.) may be used as RVSS fixtures, but shall not induce resonances which induce responses

that cause system degradation or require notching to the extent that screening effectiveness is impacted.

4. Number of Axes:

- The number of axes shall be three. The number of axes can be reduced to two when approved by NAVSEA, if justified.
- Simultaneous two or three directional stimulus, either random or quasi-random, is acceptable.

5. Duration:

- RVSS shall be applied for a minimum of 10 minutes in each axis.
- If multi axis stimulus is applied, the RVSS shall be for a minimum of 10 minutes per axis combination.

6. Performance Monitoring:

- Not required.

7. Power On/Off:

- Not required.

8. Failure Free:

- Not required.

2.4.2 RANDOM VIBRATION PROFILE

In order to obtain an optimum RVSS, it is necessary to obtain an effective random vibration profile. The principal parameters in random vibration are the number of axes vibrated, the input stimulus to the equipment, and the duration of the vibration. Due to the varying parameters of electronic hardware and the complexity of optimizing the vibration levels, there is no one profile for all equipment. The required method of determining the maximum allowable PSD levels is to calculate the input profile to the PWA on actual hardware using the methodology contained in Section 5 or similar methodology.

The values that can be determined using Section 5 for the maximum allowable PSD input level are excellent starting values. These values are calculated to establish a baseline for the vibration levels. The maximum PSD input level determined is the largest possible PSD level that the PWA can withstand in each axis due to the limitations of the worst-case part. Therefore, the maximum allowable PSD level in each axis determined by the method

presented in Section 5.3 shall be reduced by 25% before beginning any vibration proof test. If failure occurs, the proof test shall be terminated and the failure analyzed to determine if the failure was a latent defect or if the PWB/parts were overstressed. If the failure was due to latent defects, the PSD level may be raised and the test continued using screen failure analysis techniques until a plateau is reached where surfacing of latent defects is optimized, but below PWA overstressing. Once this plateau is achieved, other identical PWAs shall be tested to insure production variations in mechanical strengths do not result in overstressing a portion of the lot.

If the first proof test doesn't produce any fallout, the PWA is most likely being understressed. The PSD levels shall be raised and proof testing continued by following the screen-failure analysis technique described above. In no event shall the PSD levels exceed the maximum values determined by Section 5.3 or $.04 \text{ g}^2/\text{Hz}$.

2.4.3 Hardware to be Considered for Deletion of RVSS

- Purely mechanical hardware
- Backplanes
- Large cabinets and uncontrollable hardware

SECTION 3

PART LEVEL SCREENING APPLICATION INFORMATION

3.1 INTRODUCTION

Part screening is a process designed to remove those parts having inferior quality and hence reliability. Such screening is accomplished by subjecting a production lot of parts to various electrical, thermal, and environmental stress for the purpose of making the weak ones fail. The part level screening process must be designed to meet the following criteria:

- Test and stress levels must be carefully selected to detect inferior parts;
- Tests must be nondestructive and non-degrading to good parts;
- Testing must be adequate to screen out all potential failure mechanisms of the parts to be screened;

An effective screening program requires a detailed understanding of materials, fabrication and packaging techniques, electrical and thermal characteristics, and manufacturing tests performed on the parts to be screened. In addition, to limit costs, screening should be based upon the least amount of testing required to provide an effective screen.

Much cost and effort has been expended by DoD agencies and industry developing reliability screening processes and requirements for the major types of parts used in military equipment. These requirements have been detailed in the military specifications for these parts. Stress screening, particularly at the part level, should not develop any new or change any of the current, acceptable part level screens.

Screening levels (normally referred to as quality levels) for the three main categories of military specification parts are as follows: (1) screened military grade passive electrical parts (e.g., relays, coils, resistors and capacitors) are procurable to Established Reliability (ER) Military Specifications categorized as to ER failure rate level (normally M through S); (2) military grade discrete semiconductor devices are procurable to MIL-S-19500 and its detailed slash sheets, and are categorized as JANTX, JANTXV and JANS screening levels; (3) screened military grade microcircuits are procurable to MIL-M-38510, are labeled JAN, and categorized as to quality level (i.e., B or S).

Commercial grade, military grade, and military ER and JAN grade parts are generally physically and functionally interchangeable with the basic difference being the failure rate

levels, which can vary by orders of magnitude. ER and JAN parts have been screened per Military Test Standards by certified manufacturers as required by the specific part military specifications. Government inspectors monitor and periodically survey and recertify these manufacturers to assure that the high reliability levels of the parts are maintained from lot to lot.

In addition to the military grade ER and JAN parts, there are some parts often referred to as "vendor equivalents". "Vendor equivalent" parts have been subjected to screens/tests similar to those required by the ER or JAN military specifications, but do not meet the full requirements of the ER or JAN military specifications and may not have been screened/tested on a 100% basis. Such vendor equivalents exhibit lower failure rates than their commercial counterparts, but higher than standard military parts when both are subjected to a military environment.

The purpose of conducting a screen is to "weed out" infant mortality failures prior to incorporation of that item into its next higher assembly and/or commitment of the item to its final use. In keeping with this purpose, the selection of a cost effective screen is dependent upon many factors which include the end use environment, the part's intended life, the ease of conducting repair, any warranty provisions, and type of application. The decision process in selecting a cost effective screen involves understanding the device's failure mechanisms, then selecting a screen that will induce the failure mechanisms expected to be inherent in that device. It is desirable to perform only those screens which are cost effective to the end user during the entire life cycle.

3.2 FAILURE MODES AND MECHANISMS

In developing an effective part screening sequence, one must understand the device's construction, function, and potential manufacturing flaws with consequent failure modes and failure mechanisms of the devices to be screened. For example, Integrated Circuit (IC) failures can be attributed to chip or die related failure mechanisms that are largely dependent on the IC fabrication process and technology, and package related failure mechanisms that generally result from the assembly process.

It is important to realize that no single screen is effective in precipitating all defects. However, a series of screens can be developed to significantly reduce the probability of these defects escaping detection. Thus the selection of a screen depends on:

- The device technology, chip design, maturity, and user history.
- The expected failure modes and mechanisms.
- The supplier history (previous experience with the same part technology).

Additionally, when considering a part screening policy, one must be willing to accept the following conditions:

- Defective devices are to be expected in the population.
- The screening stress and electrical tests must eliminate or significantly reduce the population of these defective devices.
- Handling and testing must not introduce degradation or damage and must not jeopardize part life span.
- Screening procedures must be standardized and routine. New or innovative screens at the part level may end up being either noneffective to bad parts or damaging to good parts.

To achieve the requisite level of reliability, it is essential to understand the failure modes and mechanisms inherent in these devices, and then develop effective means of detecting or screening parts that exhibit these failure modes.

3.3 STANDARD SCREENS FOR DISCRETE SEMICONDUCTOR AND INTEGRATED CIRCUIT DEVICES

A number of imposed environmental stresses are used for screening defective parts from the manufactured population. The environments available to impose stresses on semiconductor materials include subjecting devices to a wide range of temperatures, applying electrical potentials, electrical currents, several forms of mechanical stress, and correlating various energy levels to specific failure modes. The specific screens are detailed in MIL-STD-750 for discrete semiconductor devices and MIL-STD-883 for integrated circuit devices.

The imposed stresses are intended to either accelerate degradation mechanisms caused by a manufacturing flaw to early failure, or otherwise reveal the existence of the defect. Ideally, the stresses do not degrade good devices. However, the stresses needed to screen for defects will likely introduce nonreversible microstructural and chemical modifications in normal materials as well. Certain of the material changes induced by some applied stresses are actually beneficial to the durability of the circuit structure. However, most stresses are more likely to produce modifications which effectively consume a small part of a device's operating life. For well designed, mature product lines and a carefully conceived stress screen, the portion of the device life consumed by the screen is minute and overwhelmingly compensated by greater reliability performance of the part.

The detailed response of part materials to the available environmental stresses is crucial to the successful application of a screen. The most common types of semiconductor and IC screens used to eliminate both die related and package related defects are as follows:

- Internal Visual Inspection (also called Pre-Cap Visual)
- Stabilization Bake (also called High Temperature Storage)
- Temperature Cycling (or Thermal Shock)
- Constant Acceleration
- Burn-In
- Electrical Test (Static, Dynamic or Functional, and Switching)
- Hermeticity (also called Seal or Leak Test [Fine and Gross])

The above screens, as applicable, are usually performed in a specific sequence to detect appropriate failure mechanisms for the end use application. Military part specifications determine the screens to be performed and the order in which they are to be performed. NAVSEA requirements for upgrade screening and their order is specified in

Table 3-1

Screened Failure Mechanisms vs. Screen

FAILURE MECHANISM	SCREEN								
	INTERNAL VISUAL	HIGH TEMPERATURE STORAGE	THERMAL CYCLING	THERMAL SHOCK	CONSTANT ACCELERATION	HIGH TEMPERATURE REVERSE BIAS	BURN-IN	ELECTRICAL TEST OVER TEMPERATURE	HERMETICITY TEST
Lifted or Broken Wires	X							X	
Lifted, Cracked, Broken Die or Substrate	X							X	
Improper Die Attachment	X		X	X	X			X	
Overbonding/Underbonding	X								
Excessive Wire Loop or Sag	X								
Metallic Contamination	X							X	
Improper Die Location or Orientation	X							X	
Foreign Materials/Particles	X								
Improper Wire Bond Attachment	X	X	X	X		X	X		
Metallization Defects	X	X				X	X	X	
Package Defects	X		X	X	X				
Die Surface Defects	X		X	X				X	
Corrosion		X							
Thermal Mismatch			X	X			X		
Intermetallic Defects		X				X	X	X	
Plating Defects		X					X	X	
Cracked Dies	X		X	X				X	
Seal Anomalies			X	X					X
Diffusion Defects						X	X	X	
Oxide Fault/Pinholes						X	X	X	
External Lead Defects						X	X	X	X

Section 2.2.1. Final electrical measurement tests must be performed after the stress screening sequence to detect device failures and ensure device conformance to specification limits over the entire operating temperature range. Since for some screens, the only means of detecting flaws is in the subsequent electrical tests. Failure mechanisms, or defects, which are stimulated by the above screens are displayed in Table 3-1.

3.4 BRIEF DESCRIPTION OF STANDARD SCREENS

Screening, the concept of applying such tests as visual examination, electrical, package leak, thermal shock, etc., can isolate many potential failures and remove them from the lot prior to insertion into the manufacturing process. Following is a brief synopsis of standard screens and tests.

3.4.1 INTERNAL VISUAL INSPECTION (PRECAP VISUAL)

Internal visual, or precap inspection is a visual inspection of the part's internal materials, construction and workmanship. It is performed immediately prior to final package seal, particularly for integrated circuit devices. It is an effective method to eliminate parts with unacceptable assembly errors and internal handling damage.

3.4.2 HIGH TEMPERATURE STORAGE (DISCRETE SEMICONDUCTORS ONLY)

The application of elevated temperature to semiconductor materials will accelerate chemical degradation due to an improper combination of materials during device fabrication or the presence of contaminants within the package or circuit materials. Elevated temperatures also relieve residual mechanical stresses within metals of the circuit. Good wire bonds can actually be improved during the bake while reactions taking place at the interfaces of poor bonds may induce them to subsequently lift off. Stabilization Bake is inexpensive because it is a batch or lot oriented stress.

3.4.3 TEMPERATURE CYCLING (OR THERMAL SHOCK)

Mechanical stresses imposed by direct thermal environments will result in abnormally high stress levels at mechanical flaw locations. Typically microcracks, hard precipitates, and abnormally thin features become stress concentrators in material structures. Thermal cycling will likely initiate mechanical fatigue degradation mechanisms in all circuit materials, but the processes will be greatly accelerated where mechanical or chemical defects have created a stress concentration. Thus the cyclical stresses created during temperature cycling or thermal shock are employed to accelerate crack growth mechanisms at such locations to produce failure during this stress screen. Temperature cycling or thermal shock is inexpensive and is performed on a batch or lot basis.

3.4.4 CONSTANT ACCELERATION

Mechanical stresses are difficult to apply directly to circuit materials for stress screening. A centrifuge can be used to impose a constant acceleration on circuit materials such that their inertial mass essentially tugs on a wire bond or a die attachment. High acceleration and inertial forces can be produced using transient mechanical shock techniques. However, due to the low density of aluminum, the forces on aluminum wires associated with reasonable values of constant acceleration are usually too small to serve as an effective screen for poor wire bonding.

Constant acceleration was effective when gold wire bonding systems were widely used for hermetic devices. With the change to aluminum wire bonding systems for most semiconductor and IC devices, the value of this screen in precipitating wire bonding problems is less effective. The screen can be effective in locating die lifting and package defects. Some devices still use gold wire bonds and can benefit from this screen.

3.4.5 BURN-IN

With semiconductor devices, the three most important failure accelerating stresses are temperature, bias voltage, and time. Increasing any one parameter tends to accelerate failures by increasing available energy to a threshold that activates various failure mechanisms.

Semiconductor burn-in is the artificial aging of semiconductor products to improve quality and insure the shipment of parts having a constant and acceptably low failure rate. Burn-in is the most effective screen in eliminating die related infant mortality failures because it takes the actual or worst case operation of the device and accelerates it through a time, power, and temperature relationship. The accelerated stress conditions are intended to activate the time temperature-dependent failure mechanisms to the point of detection in a relatively short period of time. During power burn-in, the semiconductor is operated under maximum electrical and elevated thermal conditions for a specified time, usually for 96, 160, or 240 hours.

For ICs, there are two basic types of burn-in, each of which results in a variation of the burn-in stresses created. The two types are described in Method 1015 of MIL-STD-883 as Conditions A through E as follows:

- Steady State Burn-in (Conditions A, B, or C).
- Dynamic Burn-in (Conditions D and E).

Steady State Burn-In - Steady state burn-in applies a DC bias to the device at an elevated temperature in a manner predetermined to either forward bias or reverse bias as many junctions as possible within the device. Steady state reverse bias (Condition A) burn-in is used for digital and linear circuits, mainly with NPN inputs and outputs. Steady state forward bias (Condition B) burn-in is used for linear ICs and some digital circuits, mainly

with PNP inputs and outputs. Test Condition C, steady state power and reverse bias, can be used on all digital and some linear devices.

Dynamic Burn-In - Dynamic burn-in, where dynamic parameters such as timing and status faults are continually monitored, results in higher power dissipation, current densities, and chip temperature than steady state burn-in. It is the most effective means of burning-in Large Scale Integrated (LSI) and Very Large Scale Integrated (VLSI) circuits. The two most common types of dynamic burn-in configurations are parallel excitation (Condition D), where all devices are connected in parallel and driven by the same source, and ring counter excitation (Condition E), where the devices are connected in series with the output of one device driving the input of the next.

3.4.6 ELECTRICAL TESTS (STATIC, DYNAMIC OR FUNCTIONAL, AND SWITCHING)

Electrical testing is mandatory in the screening process. Many of the defects stimulated during the screening stages can be detected during the electrical test. It is necessary to perform comprehensive electrical measurements to ensure that stress-induced defects are detected.

It is important that all of the electrical tests be performed at maximum and minimum temperatures. It is essential that parts be tested at their design maximum and minimum operating temperatures because part specifications are determined at these temperatures and any variances will not allow the part's actual parameters to be compared with the specified values. These tests are necessary to assure that defects are detected, in that some failures are catastrophic and may be detected by a multitude of tests, while other defects are only sensitive to certain temperatures, voltages, currents, or operating speeds. In a general sense, electrical testing consists of applying a sequence of inputs to a circuit under controlled conditions, observing the output sequence, and comparing it with an expected output sequence.

Static Tests - Static tests evaluate static parameters, which are defined as dc voltages, dc currents, or ratios of dc voltages and/or dc currents.

Dynamic Tests - Dynamic tests evaluate dynamic parameters, which are defined as rms or time-varying values of voltages or currents, or ratios of rms or time-varying values of voltages and/or currents.

Functional Tests - Functional tests evaluate functional parameters, which are defined as go, no-go tests which sequentially exercise a function (truth) table or in which the device is operated as part of an external circuit and total circuit operation is tested.

Switching Tests - Switching tests evaluate switching parameters which are defined as those associated with the transition of the output from one level to another or the response to a step input.

The degree of success of any part screening program is equally dependent on both the stress phase and the electrical test phase. Well designed stress tests stimulate some failure mechanisms which may only be detectable by conducting a comprehensive electrical test after the devices have been stress screened.

It is imperative that test equipment be certified and the proper software is being utilized. Out of specification test equipment has been known to damage components being tested.

3.4.7 HERMETICITY (FINE/GROSS SEAL)

Hermeticity or leak testing is a screen performed on hermetically sealed packages (those with cavities) to detect package sealing defects such as cracks and holes, improperly formed seals, and improperly sealed lids. A package is hermetic if the leak rate is small enough to maintain the desired internal atmosphere for the desired life of the part. The detection of leaks in hermetic packages and removal of them from the production lot will keep potential corrosion related defects from becoming field reliability problems. Exposure of a package to helium (fine) or fluorocarbon (gross) gases at elevated pressures provides a screening technique for the detection of leaks in a limited leak range for hermetically sealed packages.

Hermeticity tests must be performed as two separate tests. This is necessary because devices having different magnitudes of leak rates cannot be detected by one single leak test method. Fine leak test methods will not detect devices having large holes in them and gross leak test methods do not have the sensitivity to detect fine leaks. Fine leak tests must be performed prior to gross leak tests, if the fluids used in the gross leak test methods could contain particles large enough to plug fine leak holes. If a one-micron filtration system is used the order of hermeticity testing may be reversed. Other hermeticity testing methods can be found in MIL-STD-883 Method 1014. Other techniques include radioisotope fine leak, penetrant dye gross leak, weight gain gross leak, and Nid gross leak.

Fine and gross leak tests are designed to determine the effectiveness of the seal, detecting leaks ranging from 5×10^{-8} to 1×10^{-5} atm cc/sec. They screen out the defective seals that will produce latent failures when exposed to moisture or corrosive gaseous contaminants. These tests should be one of the last screens after all part handling has occurred.

3.5 ADDITIONAL PART REQUIREMENTS/PART RESCREENING

NAVSEA has instituted additional part requirements, which is also known as part rescreening, for all suppliers/repair facilities of electronic hardware for Weapons and Combat Systems. It provides additional requirements on all incoming semiconductor and integrated circuit devices as specified in Section 2.2.2 by either the equipment contractor, an independent screening facility, or by the spare/repair facility.

3.5.1 ELECTRICAL PERFORMANCE TESTS

It is necessary to perform comprehensive electrical measurements after screening to ensure that all stress induced flaws (particularly ones which cause change in performance parameters) are detected.

Electrical Performance Test Application Considerations

Many contractors and independent part screening facilities have little experience testing at the low temperature and create handling problems and false (erratic operation) reject rates which are so severe that low temperature testing is not cost effective. When low temperature testing is performed correctly, it often detects parametric drift problems not detectable by test at room or high temperatures. Testing at parts high and low operating temperatures will detect "soft failures" (e.g. parametric drift) that may not be caught with ambient testing. If a part experiences a "soft failure" at high or low testing, the part contains a defect and will fail prematurely during fleet usage unless weeded out.

Contractors (or independent screening facilities) that have experience with low temperature testing at -55°C have found that this is an effective screen. Since -55°C is a requirement, NAVSEA program managers should carefully review contractor part screening expertise to ensure they can demonstrate competency in this screen. If competency can not be demonstrated, NAVSEA should consider time phased-in implementation.

Potential problems can be in the areas of part damage due to improper handling, normally resulting from electrostatic discharge, or broken glass frit seals due to rough handling. These problems can be encountered on parts handled by the contractor as well as parts obtained from a part distributor. Most large contractors purchase their parts directly from the part manufacturer who follow ESD handling and "soft" device handling procedures. Contractors that buy parts on a low volume basis deal almost exclusively with part distribution houses. The percentage of rejects from distributor supplied parts varies over a large range. This fall-out is normally contributed to poor handling techniques. The fall-out rate is proportional to the amount of control the contractor imposes on the distributor. If proper handling techniques and ESD control are imposed on the distributors, the fall-out decreases. Contractors that impose no controls over the distributors experience the highest screening fall-out. Contractors and independent testing facilities can damage the glass frit seals on Ceramic Dual-in-Line Packages (CERDIP) if awareness of this potential problem is not recognized. CERDIPs should never be handled in partially full IC "sticks" or "tubes". The shock imparted to the CERDIP as it slides back and forth in a partially full stick can break the glass frit seals. In addition, the automatic feed (in or out) of auto-testing equipment must never allow CERDIPs to fall at an angle greater than 30-45 degrees and should incorporate shock retarding wheels to reduce impact.

When major contractors do not have the ability to handle all the additional part requirements in-house, or when a contractor is too small to have in-house screening facilities, parts are sent to independent part testing facilities for screening. The use of an independent

facility by contractors does not necessarily create handling problems that lead to part degradation. The key is to select facilities that have both the skill to screen parts and have excellent part handling techniques. If the purchased quantity of parts by device type is large, screening at outside facilities generally presents no major problem. The most difficult problem is finding a qualified facility that can do the screening in a timely manner.

Whenever a major contractor decides to perform screening in-house, there is a potential problem of software testing compatibility. The major problem is the correlation of the test programs with those used by the part manufacturer. The contractor may be using parametric test software different from the part manufacturers. It is a very difficult task to structure the dynamic and switching portions of the electrical tests. Whenever a part lot appears to have an abnormally high fall-out rate, the first area to check is the test program itself. Often it is the test program and not the parts that are at fault. This problem appears to be less prevalent in independent screening houses for two reasons. First, many times these facilities buy the software programs from the part manufacturers or from test equipment manufacturers who in turn have purchased it from a part vendor. Also independent screening facilities are less likely to allow an abnormally high fall-out rate to leave their facility without checking both accepted and rejected parts on curve-tracers, etc., to verify the rejected parts are outside the part specification requirements. However, prior to selection of an outside screening facility, a contractor should review the test programs with them. If any test correlation problem does appear to exist, the contractor can furnish the test software to the screening facility. Reputable screening facilities maintain "gold parts". A gold part is essential in exercising the test equipment and software prior to parametric testing of a part lot which is nomenclatured identically to the gold part. Once the test equipment is "checked-out" using the gold part, software incompatibilities should be nonexistent.

Considerations for Sample Electrical Performance Testing

A problem encountered with the static, dynamic/functional, and switching testing with many companies is the performance of 100 percent screening of parts that have long histories of little or no fall-out. Manufacturers should be encouraged to use their data bases to identify parts by type and manufacturer and delete or reduce rescreening on those parts that have proven track records.

After data review of on-going programs, it is estimated that about 50 percent or more of the discrete semiconductor and microcircuit lots received by major contractors are candidates for sample rescreening or the deletion of rescreening requirements. To accomplish this could require modification to existing contracts and may require a cooperative exchange of screening results by part type and manufacturer with other programs within NAVSEA.

The establishment of a contractor rescreening standard or policy should always include considerations for when it is appropriate to sample rescreen or delete rescreening on a selected group of parts. A major objection to actual implementation of part screening is

that too much time and money are spent screening good parts and too little is spent on failure analysis and corrective action to improve the problem parts.

Two major considerations must be well thought through before reduced screening should take place. Most screened date code lots will either demonstrate little or no latent defects ($< .03\%$) or a major quality problem (rejects $> 2-4\%$). There are numerous reasons for high reject rates: (1) newness of technology or length of time the device has been on the market, (2) change in location of the production facility, (3) expansion of the production facility, or (4) major change in the manufacturing processes or process monitoring equipment, etc. For example, technologies on the market less than two years rarely have a reject rate low enough to justify less than 100 percent rescreening.

Reducing the additional part requirements to a sample basis or completely eliminating the tests can be justified for some part types and/or part families. The purpose for requiring additional part screens is to guarantee, in the most cost effective manner, that parts being used in mission critical hardware are functional within specifications and reliable. In some cases the additional part requirements have been taken to extremes and the parts have been degraded by excessive handling or improper testing.

In order for parts to be guaranteed to have a uniform failure rate the part manufacturers processes must be under statistical control with minimal failures, the part manufacturer must demonstrate continuous process improvements, and the part manufacturer must have the ability to perform failure analysis and take corrective action to cure any problems or discrepancies encountered. If these steps are taken and the parts are tested to their specifications, SCD, MIL-STD, or commercial requirements, prior to shipping, the parts may be shipped directly to the end-item user and placed directly in the stock room providing that 1) there is no intermediate operation opening and/or splitting part lots being shipped and 2) the end item user accepts the product without further handling. A part distribution house is allowable providing that the parts are held in bonded stock (as defined in section 1), the lots are not split, and the original shipping containers are not opened. If the bonded stock is broken prior to the end item stockroom, the parts must be treated as untested parts and receive a complete rescreen. The reduced/deleted rescreening flow requirements can be seen in Figure 3-1. Additional part requirements that are required but have not been met at the part manufacturer must be performed by the end item user. These screens include unperformed electrical testing, PIND (if unglassivated), and DPA. The DPA requirements can be met if a precap visual was performed and documented by the part manufacturer.

Non-standard or SCD procured parts, not meeting the minimum requirements specified here-in, must still meet the upgrade screening requirements described in Tables 2-1 and 2-2. These parts can still qualify for reduced or deleted rescreening requirements providing that the upgrade screening is performed by the part manufacturer and/or qualified testing house and the parts are placed into bonded stock immediately following testing. Any tests or screens that were not accomplished by the part manufacturer and/or test house must be performed by the end-item user, e.g. DPA and PIND.

Another way to reduce from 100 percent rescreening is to achieve 100 Part Per Million (PPM) failure rate. If a 100 PPM can be achieved using a family of parts (as defined in section 1), the rescreening requirements can be deleted. Again, the parts must be shipped in bonded stock and unopened except by the end-item user. Any bonded stock opened prior to end-item user must be considered suspect and receive 100 percent rescreening.

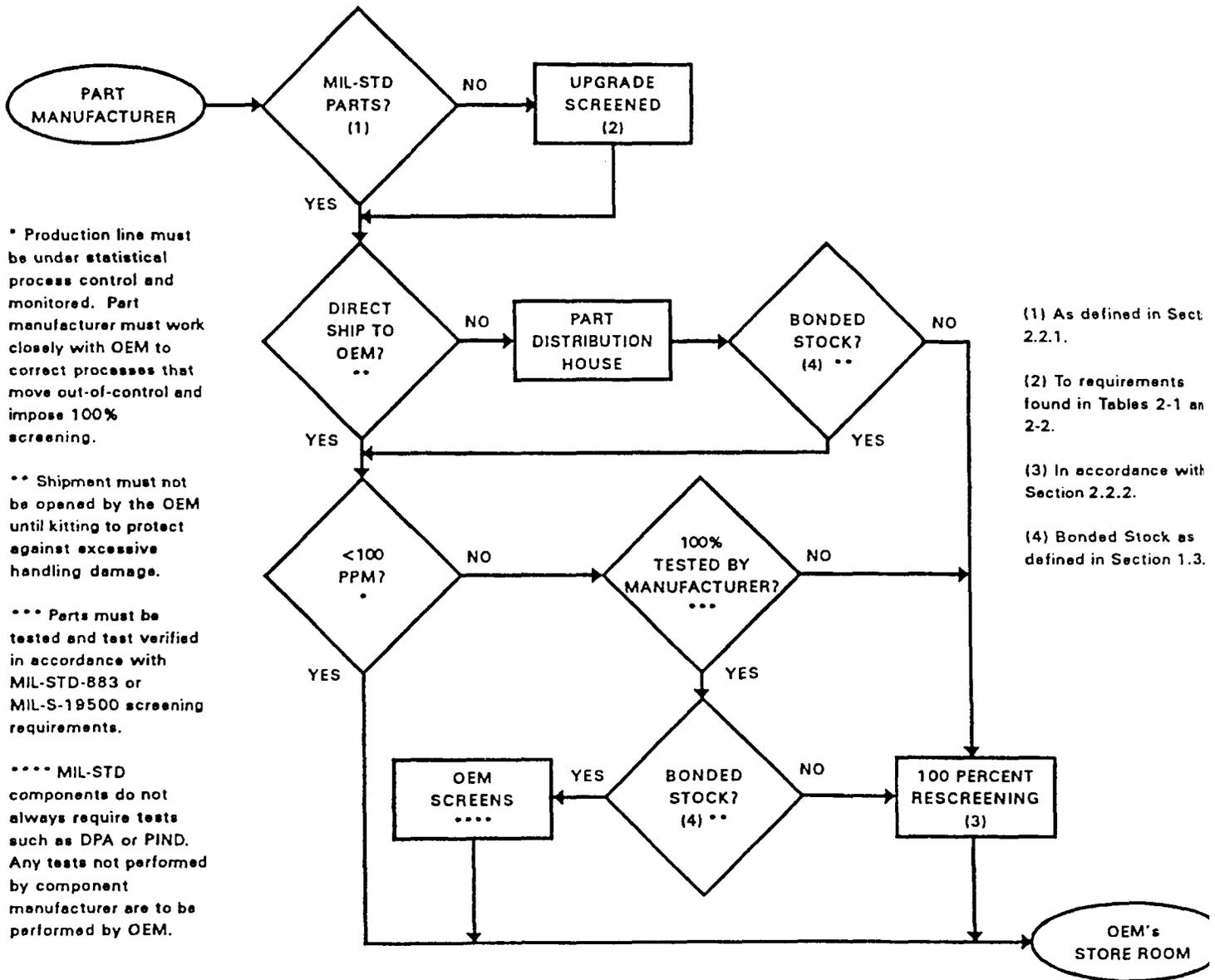


Figure 3-1 Reduction/Deletion of Additional Part Requirements Flow Chart

The Office of the Assistant Secretary of the Navy recommends a 100 PPM failure rate be demonstrated on a device before it can be eligible for sample additional part screening. Although 100 PPM failure rate guarantees high quality parts, most Navy contractors do not purchase enough parts to prove a 100 PPM failure rate with any degree of confidence. Therefore, other techniques must be available to reduce rescreening requirements on known good parts and not reduce the part or equipment's reliability. The Procuring Activity must be involved in the decisions to reduce rescreening. The Procuring Activity must also review and approve the criteria used to statistically prove 100 PPM.

When developing justification for reduced screening, contractors should as a minimum institute the following:

1. Develop a data base that will identify parts that can be sample screened/no rescreening versus 100 percent screened. A dynamic plan must be developed. Correlation of sample screened/no rescreening lots with manufacturing part failure data is critical.
2. Establish threshold levels for maximum number of defects from the sample electrical screening that will trigger a failure analysis and 100% screening of that lot. A sample size should be at least 60 devices. Unless the contractor is consuming, in the production process, a large quantity of the same device type, the set-up and minimum lot size charges associated with 60 devices may make sample screening economically unfeasible. If any failures are noted during electrical testing, the entire lot should be a candidate for returning to a 100% screen. Latent defects tend to be lot related. The percent defective will normally be very low (<.03 percent) for a good quality lot, or high (>2-4%) indicating a lot quality problem.

A reduced screening program is a cost-effective alternative to 100% rescreening. Under most circumstances, the cost to screen would not be considered a factor for reduce screening because rework cost savings at the assembly level should offset the cost of 100% screening. However, stringent screening requirements established at the beginning of a production program may not be cost-effective in the later manufacturing stages. As a production phase progresses, the effectiveness of already established tests and the conscientiousness of part suppliers are factors in the consideration of continued 100% rescreening of specific parts. An inherently simple part from a good supplier may not require 100% rescreening throughout the entire production cycle, while a complex device from a careless manufacturer may show a significant cost savings with 100% rescreening throughout the life of a program. If a supplier consistently provides a reliable product, there may be justification to reduce or delete the rescreening requirements. Also, while parts purchased as Class B JM38510 and JANTX MIL-S-19500 have a less chance of rejection than parts upgrade screened to an equivalent, there is no reason to handle these upgrade screened parts differently than Class B and JANTX parts when it comes to reducing rescreening.

3.5.2 PARTICLE IMPACT NOISE DETECTION (PIND)

Particle Impact Noise Detection (PIND) is a process of vibrating a part and using acoustic noise pickup devices to check for loose particles inside a hermetic sealed cavity package. This test should be accomplished on all unglassivated devices that might be shorted by loose conductive particles. If DPA is accomplished prior to PIND, all unglassivated lots will have been identified. Part manufacturers' process data can also be used for justification not to PIND parts. If the manufacturer's process identifies glassivation in the manufacturing process and the manufacturer certifies the parts to the workmanship requirements, the parts can be considered glassivated. PIND screening is performed by placing a device on an acoustic transducer which is located on a vibrating shaker head. While vibrating the part, the acoustic pickup device listens for loose particles inside the device cavity. Three simultaneous detection methods are used in performing PIND screening:

- a. Visual (oscilloscope) display
- b. Auditory detection by acoustic amplified noise, and
- c. Visual detection by means of a triggered red light for devices whose noise spike level exceeds a preset threshold level.

PIND screening apparatus in use today is capable of detecting 1 mil particles in a cavity type device. The screen is normally performed by vibrating the device at a 10 to 20 g acceleration level at a frequency of 60 and 250 Hz. A simultaneous co-shock pulse of 300 to 1800 g's is applied to jar loose any statically or mechanically held particles.

Areas for consideration when using this screen are:

- a. Inability to distinguish between conductive and non-conductive particles. Nonconductive particles may not be detrimental.
- b. The mass of the foreign particle is the controlling factor rather than its physical size.

PIND Application and Tailoring Considerations

Military contractors tend to resist PIND testing. The objections to PIND are the low through-put rate and fear of a high false reject percentage. However, most of the semiconductor and IC cavity devices being processed today are glassivated by the manufacturer. This process obviates the need for PIND testing. On most programs, less than 5 percent of the discrete semiconductors and microcircuits are not glassivated. If DPA is performed prior to PIND testing, the results of the DPA will provide positive determination of whether the device type is glassivated. This normally relieves any concern regarding through-put problems. If for some reason, a high production rate program has a

high percentage of unglassivated cavity devices, automatic feed PIND testers are available to aid in any through-put problems.

The fear of false rejects is unfounded. In many cases, parts with high PIND reject rates will have high reject rates during electrical tests. Most false reject rates are caused by improper testing techniques and lack of PIND testing experience. Sometimes coupled with the argument of false rejects is that PIND testing fails parts with conductive and non-conductive contamination, and nonconductive contamination does not necessarily represent a reliability risk to the Navy. NAVSEA requirements are to reject all unglassivated devices that fail PIND testing whether the contamination is conductive or nonconductive for two specific reasons. First, to further screen a contaminated device to determine if the contamination is conductive or not, would require a specialized screen (e.g. X-ray examination) that is moderately expensive and can have poor results in detecting conductive materials. Secondly, and of equal importance, contamination is an indication of process control problems by the part manufacturer. PIND testing is one method the Navy has of increasing its assurance that parts built with process control problems do not end up in the Fleet. Tests have also shown that large non-conductive particles can damage internal wire bonds and dies reducing the reliability of the parts.

Since PIND testing is required by NAVSEA on all hybrids, it has been recommended by some hybrid manufacturers that a "getter" material be added to capture particles during the application of PIND testing since hybrids are too expensive to discard for non-conductive contamination. However, getters may outgas (depending on the getter material), and eventually cause internal corrosion of metallization areas, wire bonds, etc. In short, getters may cause more long term reliability risk than the particle. The use of getters should receive careful evaluation and requires NAVSEA approval.

A specialized screen can be utilized known as a Conductive Particle Detection (CPD) Test. This test has been designed for the detection of loose conductive particles in packaged ICs and hybrids. The part is vibrated while electrically biased. Monitors detect changes in operating current and/or output voltage due to conductive particles striking portions of the circuit or chip surface. This is an expanded form of PIND testing, and should be the one method of acceptance for "noisy" hybrids which are suspected of containing non-conductive particles.

PIND testing is normally performed on discrete semiconductors, microcircuits, and hybrids. In addition, PIND may serve to precipitate failures in relays in that they are also cavity devices. Impact noise occurring during relay PIND testing which is regular or periodic in the noise spectrum should be ignored as a natural contact bounce response of the relay. Irregular or non-periodic noise should be investigated. PIND on relays can be performed in accordance with MIL-STD-202, Method 217.

Occasionally parts are used whose construction prohibits PIND testing. Oscillators with loose ceramic beads in the cavity are a prime example. These part types should be removed from any PIND testing considerations.

3.5.3 DESTRUCTIVE PHYSICAL ANALYSIS (DPA)

DPA is extremely useful in identifying potential defect mechanisms through visual examination and destructive testing. DPA is the process of inspecting, testing, and disassembling a device for the purpose of determining conformance with applicable design requirements and a previously established baseline after the parts have been fabricated. This systematic inspection of design, construction, and workmanship reveals weaknesses or nonconformances in materials or process changes which could ultimately cause failures. Because it is destructive, DPA is performed on a small, representative sample of a lot. Results of the sample inspection form a baseline for acceptance or rejection of the entire lot. If anomalies are found, acceptance of the lot may depend on the performance of additional tests or screens in order to remove defective devices, beyond those delineated in Section 2.2.2.

Every test or examination attempts to determine the quality of a specific production process or operation. DPA is conducted in a specific order in such a way that a minimum of data for a subsequent inspection will be affected by any previous inspection.

DPA Application and Tailoring Considerations

DPA is potentially one of the most important additional part requirements for the Navy. DPAs can eliminate parts that would escape all other screens but be a long term reliability risk. However, DPAs can be expensive and can tax the resources of a part failure analysis facility. Consideration may be given to waiving the requirement for high cost parts or small lot sizes, if approved by NAVSEA.

The DPA process can lose some of its cost effectiveness unless it is first in the incoming part testing process and is completed before any other screens commence. The importance of performing the DPA first is threefold.

First, it is preferable to wait for the DPA results prior to doing the balance of the additional part requirements (Electrical and PIND), thereby not incurring the screening costs for a lot that will be rejected. Secondly, if the DPA should detect a latent anomaly in the lot, any additional screen to remove parts with that specific anomaly can be incorporated in the remaining screening process. And last, the DPA process is the best positive indicator of whether the lot is glassivated. Note that except for hybrids, PIND testing is performed only on those cavity devices that are not glassivated. The only disadvantage in performing the DPA first is it adds to the lead time required between the time the lot is received and the time it is available for kitting on the production floor. Even with these potential production delay problems, the DPA is one of the most important additional part requirements.

Consideration can be given to performing the DPA after the electrical and PIND testing if the contractor is willing to accept the disadvantages associated with such a decision. All the advantages of performing the DPA first, as stated in the above paragraph, become disadvantages when the DPA is performed concurrently or after the other additional screens.

There is, however, a redeeming consideration to performing DPA last. DPA can use failed devices from the electrical or PIND testing and not require the destruction of a good device that would have been acceptable. By using a failed device, the statistical chance of discovering a lot-related defect may be greatly enhanced. However, one must be careful not to project a unique defect in a failed device as a lot related problem unless the defect noted and other data from that lot's additional part requirements program justifies such a projection.

When a contractor or subcontractor discovers a problem through DPA, too often a judgment is made that the defect is minor and the lot is used as is. The Navy is rarely involved in the decision making process. The contractor, or in some cases a subcontractor, may not be contractually required to have a Material Review Board (MRB) and may make the decision on their own. If the DPA results are sent to MRB, a qualified part reliability person from the Navy may not be involved. The best solution is to require prime contractors to make DPA reports a deliverable from their subcontractors and have those reports along with their own available for Navy review.

There are tailoring considerations which can be considered while performing DPAs that are worthy of notice. First, NAVSEA and contractors need to examine the requirement for DPA on all lots and consider performing DPAs only on high risk parts and/or high risk vendors. For mature technology of JANTX and Class B or above devices with a good-quality history, contractors should consider discontinuing DPAs if the data justifies such a decision. Small quantity part types are also a candidate for waiving the DPA requirement during production. Small quantity should not be used as justification during FSD. The contractor should consider expanding DPA requirements without having to be directed to do so when it is warranted. For example, when parts are identified to be a reliability risk from such things as moisture content, chemical contamination, or surface impurities, an expanded DPA is in order. This might result in a DPA requirement to include a Residual Gas Analysis (RGA) test, or a Surface Impurity Analysis. In addition, defects in the construction of ceramic (CKR, MIL-C-39014) and solid tantalum (CSR, MIL-C39003) capacitors continue to plague many production contracts. Consideration of problem part types for DPA should include these and other passive parts as well. If approved by the Procuring Activity, DPA may also be deleted if the parts have received a precap visual inspection in accordance with MIL-STD-883 Method 2013 or 2014.

3.6 EVALUATING THE EFFECTIVENESS OF ADDITIONAL PART REQUIREMENTS

The presence or absence of failures is not necessarily indicative of the effectiveness of additional part screening. The basic NAVSEA requirement is to perform additional part screening of semiconductor devices and integrated circuits. Any additional part screening program should include some of the following:

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1. Identifying the root causes for part failures is the first critical step for taking corrective action. Contractors rarely do failure analysis on parts rejected by part level screening programs. During FSD, lot related problems and/or excessive reject rates of new technology parts and upgrade screened parts should result in the contractor working with the part manufacturer to develop corrective action. These types of part problems during FSD will still exist when the production milestone is reached unless corrective action is taken. Its easy to blame the part manufacturers for the part problems and overlook the contractor's obligations to procure good parts and take corrective action when part problems are discovered.
 2. Subcontractors should comply with Item 1 and report all failure analysis and DPA results to the prime contractor. To ensure a proper failure analysis, the prime contractors may perform the failure analysis for smaller subcontractors.
 3. Part yield rates, failure analysis and DPA results should be agenda items for failure review boards, program reviews, or other activities that involve Navy overview.
 4. A total and comprehensive Part Management Plan should be developed. This plan, as a minimum should address Items 1, 2, and 3 above. The potential exists for gaining a wealth of part information, thus providing economic and technical justification for effective tailoring. Maximum utility can be obtained by recording appropriate information on part failures/discrepancies at incoming inspection, during manufacturing, TCSS, RVSS, all the way through final system acceptance test. A significant amount of this type of information is already recorded by a MIL-Q-9858 program and a Failure Reporting, Analysis, and Corrective Action System (FRACAS) which is normally a contractual requirement. A comprehensive Part Management Plan ensures that an organizational element will monitor/track part failures from the time the part enters the contractor's facility until such time that the part leaves the contractor's facility. This same organizational element (e.g. Q.A., Reliability Engineering, etc.) would then have the necessary data for recommending effective tailoring.

SECTION 4

THERMAL CYCLING STRESS SCREENING APPLICATION INFORMATION

4.1 INTRODUCTION

The least controversial and least resisted portion of the ESS program is Thermal Cycling Stress Screening (TCSS). Problems that arise are usually matters of interpretation of the requirements or implementation techniques, rather than whether or not the screen is cost effective. The Printed Wiring Assembly (PWA) level thermal cycle is very cost effective. Most contractors that have collected data have found that this screen more than pays for itself in the manufacturing process. Higher indenture level thermal cycling is also cost effective, particularly to the Navy.

As the design process matures, design problems will diminish significantly and should approach zero. Thermal cycling at the end of a hardware development program and throughout the production program should show minimal design problems, with workmanship and parts problems predominating. Thermal cycling with good parts and packaging techniques is not degrading even with several hundred cycles. However, the packaging design must be compatible with the temperature range or the yield will be reduced and/or good hardware will be damaged. This compatibility is established by temperature range testing the hardware during Full Scale Development (FSD).

For development or new production, it is required that thermal cycling be done twice, once at the PWA level and secondly, thermal cycling with performance monitoring at the lowest possible indenture level above the PWA. For reprourement, spares, and repair, one level of TCSS is required per Section 2.3.2, paragraph 3.

4.2 TEMPERATURE RANGE

For the majority of PWAs, the following starting values for temperature range can be used: the low limit of temperature range should not be set below the highest low-rated temperature part, and the high limit should not be set above the lowest high-rated temperature part. The required temperature range (ΔT) is 120°C.

For higher indenture levels, the equipment storage specification minimum and maximum temperature limits should be used to establish the overall range. Most parts will withstand temperature cycling with power off through a storage temperature range of -55 to 100°C. The maximum safe range and the fastest rate of change of hardware temperature provide the best screening.

One potential problem that must be considered is thermal overstressing parts. If PWAs contain commercial grade semiconductors rated at 85°C, the equipment should not be thermal cycled above 85°C. The upper temperature limit during higher indenture level testing must be below the point of overstressing parts.

However, for most PWAs built using parts that are designed to operate over the full military temperature range, the recommended temperature range (ΔT) of 120°C presents no problems. Temperature ranges for the next higher assembly (module or unit) should be as close as possible to the PWA level without overstressing any internal parts.

4.2.1 TEMPERATURE RANGE VS. SCREENING EFFECTIVENESS

Review of various screening programs demonstrated that the temperature range (ΔT) is a significant factor in determining screening effectiveness. Holding all other thermal cycling parameters constant (rate of change, number of cycles, thermal profile, etc.), the larger the temperature range, the more effective the screen is in reducing the number of cycles required to remove defects. If the number of cycles is relatively small (5-10 thermal cycles), the temperature range (ΔT) can significantly change the effectiveness of the screening. Increasing the range beyond 120°C has not generally proven to be effective and may be degrading to good hardware. It has been shown that, reducing one TCSS parameter can be compensated for by an increase in one or both of the other TCSS parameters.

4.3 TEMPERATURE RATE OF CHANGE

The temperature rate of change of individual electronic parts depends on the chambers used and the size and thermal mass of the hardware. In general, the rate of change of internal parts should fall within 5°C/minute and 20°C/minute, with the higher rates providing the best screening. At the PWA level, the temperature rate of change must be measured by a thermocouple mounted directly on the electronic part with the largest mass (excluding magnetic devices and connectors), or at a worst case (slowest) non-metallic portion of the Printed Wiring Board (PWB). The rate of change requirements are specified for the fastest transition rate achievable either on the hot to cold side or the cold to hot side. The rate of change for the slow side must be driven as hard as possible by the screening equipment.

Measuring the temperature rate of change on the largest mass part need only be performed once for each PWA as a hardware proof test. Once the correlation in the rate of change between the electronic parts and the chamber air temperature is known, PWA thermal cycling during production need only monitor the temperature of the chamber air, or any other convenient location. This alleviates the need for multiple thermocouple monitoring when thermal cycling a large number of PWAs at one time. The hardware proof test must, however, use the same chamber characteristics as the production chamber. In addition, the proof test must account for the maximum thermal load of a full chamber of PWAs based on anticipated TCSS implementation.

The expected load should be thoroughly profiled to determine the actual response of the PWAs. The thermocouples used to profile the responses must be insulated from the chamber air to ensure that the actual response is measured, not the chamber air.

A check of most thermal cycling programs currently used indicates that for an indenture level higher than PWA, temperature rates of change (i.e., 5°C/minute) are chamber air temperature rather than temperature rate of change of the cold plate (as defined in section 1). Because of thermal time constants, it is likely that temperature rates of change actually experienced by the electronic parts probably are no greater than 1 or 2°C/minute when chamber air temperature is monitored at 5°C/minute. The temperature rate of change must be determined based on either the cold plate or largest PWB surface temperature. This can also be established through a hardware proof test. Once the correlation between cold plate and chamber air temperature is known, the actual TCSS may be performed by monitoring only chamber air temperature rate of change. At higher indenture levels, temperature rates of change must be greater than or equal to 5°C/minute. This is normally limited by environmental test equipment capability.

Controlled "overshooting/undershooting" of the chamber air temperature allows the use of thermal chambers with limited capability, or can substantially increase the temperature rate of change for large thermal loads. Overshooting/undershooting is a method of achieving an increased temperature rate of change by allowing the chamber air temperature to exceed the upper and lower screening temperature limits for a controlled period of time. The "overshooting/undershooting" condition is then removed before the item under test reaches its thermal limit as demonstrated in Figure 4-1. Controlled overshooting/undershooting is permissible and encouraged as an excellent method of achieving higher temperature rates of change, thereby increasing screening effectiveness. The key word is "controlled". A determination must be made on the impact the overshoot has on the part with the smallest thermal mass. The consideration of placing a thermocouple on the smallest thermal mass part will ensure that it is not overstressed. Also, the thermal limit of the PWB material must be considered and controlled.

4.3.1 TEMPERATURE RATE OF CHANGE VS. SCREENING EFFECTIVENESS

The effectiveness of any TCSS is a function of various parameters that comprise the thermal cycling screen. The rate of temperature change has the most significant effect on the screen and is best evaluated when all other parameters are held constant. For example, changing the higher indenture level screening from 5°C/minute to 15°C/minute on radar equipment in production resulted in the reduction of higher level in-house test failures by 25 percent.

4.4 NUMBER OF THERMAL CYCLES

In the past, the number of thermal cycles has varied from a low of 2 to a high of 168. The number of cycles was selected based on module complexity. Authorities now agree that

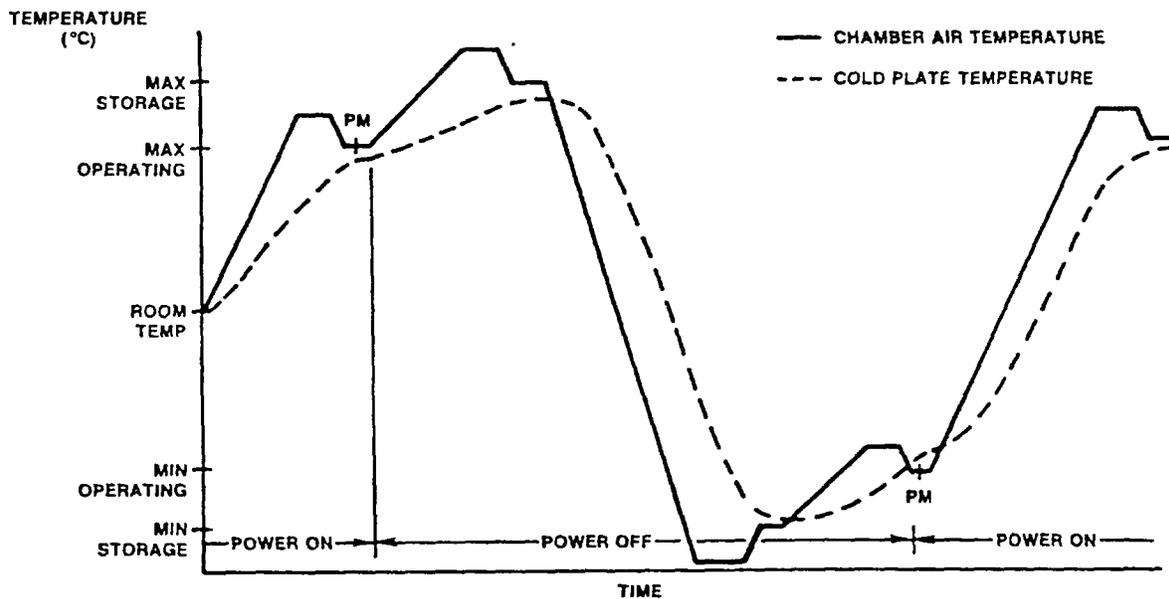
a number of cycles should not be based on parts count, i.e., complexity, but on the thermal parameters associated with the hardware being screened.

NAVSEA's approach to establishing the required number of cycles for a particular TCSS program is to establish a lower limit on the number of thermal cycles, and increase the number of cycles based upon:

- a. Reduced rate of temperature change ($^{\circ}\text{C}/\text{minute}$)
- b. Reduced temperature range (ΔT)

Reductions in temperature range and rate of change are necessary when the equipment is unable to withstand the larger ΔT or the thermal cycling equipment is unable to change the temperature rate as quickly as desired.

A reduction in the number of thermal cycles may be justified if screening data demonstrates that an insignificant number of latent defects are stimulated after a certain point when TCSS is performed in accordance with the requirements of this document.



PM = PERFORMANCE MONITORING

NOTE: STRAIGHT LINE GRAPHS FOR CHAMBER AIR TEMPERATURE ARE IN REALITY ROUNDED IN AN EXPONENTIAL MANNER.

Figure 4-1 Example of Chamber Air Thermal Overshooting/Undershooting

4.5 FAILURE FREE CYCLE

When thermal cycling is used as a stress screen, it is standard practice to allow repairs/rework without requiring a repeat of the entire screen. Some ESS programs have not required failure free cycles, some have required the two final cycles to be failure free, and some programs have required as many as 20 consecutive failure free cycles. NAVSEA's requirement emphasizes that the last cycle be failure free without repeating the entire screen. This allows for a very cost-effective approach to TCSS. In most cases, contractors perform the entire PWA level TCSS program without any performance monitoring. Failed PWAs are repaired/reworked and a maximum of two individual and separate failure free cycles are imposed on the PWA when subsequent TCSS at a higher indenture level is not performed. If higher indenture level TCSS is performed after the PWA level TCSS, the failure free cycle must be imposed at the higher level.

Experience has indicated that a mandated failure free thermal cycle may be deleterious to some PWA's that continue to fail. Normally in situations just described, the PWA continues to fail because a replaced part continues to fail, and the rework costs become uneconomical and quality control standards become difficult to be maintained. In recognition of this observation, a corrective action or alternative method must be proposed to eliminate the continuously failing PWA. Examples of corrective action include changing part types, design changes, and manufacturing or process changes. Examples of alternative methods include TCSS without that particular part and designing a special screen for that part prior to PWB insertion.

4.6 PERFORMANCE MONITORING AND POWER ON/OFF CONSIDERATIONS

One area of TCSS which still requires some additional consideration is in the area of whether performance monitoring (as defined in section 1) should be required during the screening process, and when power on/off should be invoked. These considerations are primarily differentiated by two factors:

1. Without performance monitoring, intermittent failures may go undetected (argument for performance monitoring thus requiring power on).
2. With power on, the parts may not be able to be cycled over a large temperature range without overstressing some parts (argument for power off).

An important question to raise during higher indenture level TCSS revolves around whether it is necessary to monitor hardware performance while thermal cycling is being applied. This concern stems from the traditionally limited availability of electrical test equipment and the conflicts thus generated between screening and bench test operations. In addition, schedules may be further affected by the need to move and set up test equipment at each different location. Before making the decision not to monitor performance while

applying TCSS, it is important to appreciate the risk involved in terms of defects that may remain undetected.

If all of the failures that occurred were "hard" failures, performance monitoring might not be necessary. (The term "hard" failure refers to those failures that "stay failed" once they occur, even after exposure to stress conditions has ceased.) Unfortunately, many failures that occur in electronic hardware are "conditional" failures (intermittent failures). That is, they can only be detected while the thermal stress is being applied. Once the environmental stress is removed, the "failure" disappears.

It is required that higher indenture levels being thermal cycled be performance monitored at the lowest equipment operating design specification temperature limit (usually 0°C for Naval Sheltered Equipment) and at the upper temperature limit (usually 50°C) during the positive increasing portion of the thermal cycle. Performance monitoring at these temperature limits will surface intermittent defects that would go undetected at room temperature. For higher indenture levels currently in production, performance monitoring and power on/off thermal cycling is still preferred. It is often impossible, however, if test equipment has not been developed, to power the equipment at an indenture level low enough to perform cost-effective thermal cycling. Generally, the decision of whether or not to screen with performance monitoring and power on/off for these programs is based on the cost of adapting or developing test equipment to accomplish this, and not on the maturity of the production program.

Performance monitoring should be performed in a cost effective and technically efficient manner. The use of performance monitoring is an effective technique for screening, but should not be so extensive that the cost effectiveness or screening effectiveness of the screen is affected. In cases where performance monitoring will take an excessive amount of time to accomplish, alternate techniques should be reviewed and incorporated. This decision should be jointly made by the equipment manufacturer and the Procuring Activity.

A minor problem that occurs is interpreting the power-on requirement as meaning power must be on all the time during the thermal screen. Very poor screening decisions can result from this misunderstanding. For programs in Full Scale Development, test equipment and test plans must be designed with power on/off cycling as a requirement at an indenture level above the PWA level. Power on/off cycling can be combined with thermal cycling for maximum results. It is strongly recommended that power be off during the cooling portion of the thermal cycle, and during any portion that is above or below the equipment operating specification limits.

4.7 SPECIAL THERMAL CYCLING CONSIDERATIONS

4.7.1 MAGNETIC DEVICES

Magnetic devices continue to be a problem area for TCSS. Poor quality magnetics can have a high fall-out rate from TCSS. The problem is the magnetics are not effectively screened at the PWA level because the magnetic's temperature rate of change lag the rate of change of the rest of the parts by an excessive amount. A piece of equipment that, excluding the magnetics, can reach thermal stability in 15 minutes may take several hours for the magnetics to reach thermal stability. The dwell time at the temperature extremes is normally set for the smaller electronic parts and not for the magnetics.

There is an alternative screen. Magnetics should be built to MIL-T-27 and should be subjected to the optional MIL-STD-202 thermal shock screen on a 100 percent basis. Data supports that thermally shocked magnetics have little or no additional fallout with subsequent equipment thermal cycling. Thermally shocking magnetics has for sometime been a recommendation for power supply reliability and is a specification requirement for the Navy's Standard Power Supply Program.

4.7.2 WATER COOLED POWER SUPPLIES

Power supply thermal cycling has presented some unique problems. There have been several cases of power supplies being thermal cycled while mounted on water cooled cold plates. This means that the unit cannot be cycled to temperatures much below 0°C or the water in the cold plate will freeze. Worse, the water stabilizes the internal temperature of the unit which means the electronics are not actually experiencing the thermal cycling.

A better alternative is to perform most thermal cycling on power supplies without the water cooled plates. In many cases, power can still be applied, but care must be taken not to cause degradation by thermally overstressing the parts.

These same guidelines should be followed for non power supply water cooled hardware.

4.7.3 POTTED MODULES

There are many questions about the value of thermal cycling of potted power supplies and modules. Most questions arise out of a lack of understanding. Thermal cycling must be accomplished prior to potting (so that repair is feasible and to insure adequate screening parameters). Power must be off if the potting compound provides electrical insulation or a better thermal path than convective air.

SECTION 5

RANDOM VIBRATION STRESS SCREENING APPLICATION INFORMATION

5.1 INTRODUCTION

The least understood portion of an ESS program is usually the Random Vibration Stress Screening (RVSS). The problems that have arisen in the past are due to various factors including misinformation and improper techniques in determining proper vibration levels. Using previous NAVSEA Statements of Work, many contractors have used $.04 \text{ g}^2/\text{Hz}$ as an input Power Spectral Density (PSD) and in this process have, on occasion, overstressed or understressed the equipment being screened. The technique described below is just one technique that may be used to develop vibration screening levels. Other techniques are available and can be used with Procuring Activity approval.

The best screening sequence for electronic hardware is to perform a Printed Wiring Assembly (PWA) level Thermal Cycling Stress Screen (TCSS) before random vibration, and a higher indenture level TCSS after random vibration. The TCSS prior to RVSS prestresses potential defects which can then be surfaced more efficiently by RVSS. RVSS can also condition some defects just to the point of failure and a subsequent TCSS with performance monitoring completes the defect identification.

The number of axes to be vibrated is three. RVSS programs which apply vibration in less than three axes can result in a benign screen due to part rigidity in the applied axes. The number of axes can be reduced to two with NAVSEA approval if technical and economic justification can demonstrate and substantiate such a decision. An analysis must be performed in each of the three major axes to determine if any potential overstress conditions exist. It is important to note that an overstress takes useful life out of equipment but may not be visible or result in an immediate hard failure. For the methodology presented herein, a three-axes designation will be used; that is x, y, and z. The z axis is perpendicular to the PWA while the y and x axes are the lateral directions.

5.2 DURATION

The duration of an RVSS is an important factor that can be overlooked. An RVSS program which controls only the input profile can cause fatigue damage if the RVSS duration is too long. However, for a properly conceived RVSS that determines and controls the input profile, fatigue is of little concern for the duration times required. The requirement for ten minutes in each axis is derived from studies that demonstrate maximum screening effectiveness is obtained in eight to ten minutes.

5.3 GENERAL PROCEDURE

To get the best results from a screen, a simple engineering analysis must first be performed. This engineering analysis is presented in detail in Section 5.4. In order to develop the maximum allowable screening strength for each individual PWB, an analysis must be performed on each unique PWB type. Section 5.4.1 or some other engineering analysis approved by NAVSEA should be used for each PWA type. Once the allowable stress for the PWA is known, a look at the parts is necessary to determine the suspect parts in each axis to be screened. Section 5.4.2 covers most of the standard part types. If a unique part type is used, the analogy that best models the unique part should be used to obtain the estimated maximum screening level.

When reviewing the PWA for suspect parts, the following guideline should be used; in the Z axis (perpendicular to the PWA surface) large ICs and LCCs mounted centrally on the PWA surface, large tombstone type capacitors, and large axial lead components should be analyzed. When reviewing the lateral motion, large axial lead components and large can transistors should be analyzed.

One easy method that can be used to correlate the vibration data is to develop a matrix that shows the maximum allowable PSD level for each analyzed part, and the axis that was used for the calculation. Once the matrix is complete, simply use the smallest maximum allowable PSD level in each axis to determine the maximum input level that can be used to develop the screening profile.

5.4 ACCELERATION SPECTRUM

In the past, the acceleration spectrum was usually defaulted to the PSD level shown in Figure 2-3(b) commonly known as the NAVMAT profile. A technique has been developed by NAVSEA and takes into consideration the parameters of the Printed Wiring Board (PWB) and the parameters of the parts most susceptible to overstress. This technique computes the maximum allowable PSD level in each of the three axes. The methods presented in Section 5 can be used on any part that resembles the part described. The parameters needed to begin this technique are: the length of the long side of the PWB or thermal plane in inches (designated as a), the length of the short side of the PWB or thermal plane in inches (b), the thickness of the PWB or thermal plane in inches (t), the weight of the PWB or thermal plane in pounds (W), and the type of supports (fixed, free, or simply supported) for the PWB or thermal plane during RVSS. With these parameters and the following equations, the natural frequency of both the PWB and the thermal plane (if any exists) and their maximum deflections can be calculated. If vibrating in an axis other than perpendicular to the PWB's surface, section 5.4.1 through 5.4.2.4 may be omitted.

5.4.1 MAXIMUM ALLOWABLE PSD LEVEL OF THE PWB

The natural frequencies (f_n) of the PWB and the thermal plane must be calculated if hardware does not exist, or measured if hardware does exist. If a thermal plane exists, the

expected deflection (δ_{ex}) and the maximum allowable deflection (δ_{max}) of the PWB and thermal plane must be calculated and compared. The first step in determining the expected and maximum allowable deflections is to calculate the natural frequency of the PWB and the thermal plane. The natural frequency equations are shown in Appendix A with the material properties located in Appendix B. Once the natural frequency of the PWB and the thermal plane have been calculated or measured, calculate the expected G-level that the board and thermal plane will experience. Using the Crandall Equation shown as 5-1, and the input profile of Figure 2-3(a) as a starting reference $\omega_0 = .04 \text{ g}^2/\text{Hz}$), the equation can be reduced to Equation 5-2. The G-level can be placed into Equation 5-3 and the expected deflection of the PWB or thermal plane calculated. The expected deflection of the PWB or thermal plane is the largest deflection that the board or plane will see during a vibration screen using the input profile of Figure 2-3(a).

$$G = \left[\frac{\pi}{2} f_n \frac{3}{2} \omega_0 \right]^{\frac{1}{2}} \quad \text{Eq. 5-1}$$

$$G = \frac{1}{4} f_n^{\frac{3}{4}} \quad \text{Eq. 5-2}$$

and

$$\delta_{ex} = \frac{9.8 \times G}{f_n^2} \quad \text{Eq. 5-3}$$

If a thermal plane is present, the expected deflection for both the PWB and the thermal plane must be calculated with the smaller value of the two used for the remainder of this section. The smallest deflection between the PWB and the thermal plane is used since they bend together and the one with the smallest expected deflection will generally dominate during vibration.

The maximum allowable deflection (δ_{max}) of the PWB and the thermal plane must be calculated next. The maximum allowable deflection is the largest distance that the PWB or thermal plane can deflect without damaging the material properties. The maximum allowable deflection formula is shown as Equation 5-4. If a thermal plane exists, the maximum allowable deflections of the PWB and the thermal plane are compared and the smaller of the two values is used to calculate the maximum allowable PSD level for the PWB thermal plane combination.

$$\delta_{\max} = \left[\frac{F \times \sigma_{\max}}{E} \right] \frac{b^2}{t} \quad \text{Eq. 5-4}$$

where: σ_{\max} = Endurance limit (Se) of the PWB or thermal plane, psi.
E = Modulus of elasticity, psi.
F = .208 if PWB short sides are simply supported.
or F = .062 if PWB short sides are fixed.

* If one or more sides are free, use the F value that most represents the PWA fixturing.

The maximum input PSD level for the PWB and thermal plane can be calculated from Equation 5-5 using the smaller of the two expected deflections and the smaller of the two maximum allowable deflections. The maximum input PSD level is the maximum level that the PWB and the thermal plane can withstand without structural damage. The level that is calculated in Equation 5-5 is normally an extremely high value in that it represents a calculation of the maximum input level the PWB material can withstand. DO NOT ATTEMPT TO USE THIS AS AN INPUT VALUE UNLESS IT IS THE LOWEST VALUE FOUND, IN THE Z AXIS, AFTER THE PARTS SECTION (SECTION 5.4.2 THROUGH 5.4.4.2) HAS BEEN COMPLETED.

$$PSD_{\max} = \left[\frac{\delta_{\max}}{\delta_{\text{ex}}} \right]^2 \times .04 \frac{g^2}{\text{Hz}} \quad \text{Eq. 5-5}$$

5.4.2 MAXIMUM ALLOWABLE PSD LEVEL FOR PARTS DUE TO PWB BENDING

The bending motion of PWBs due to applied random vibration tends to lift the leads of the longer length parts off the board (such as ICs and larger axial lead parts). This can cause various forms of lead damage to the parts if the PSD input level is not controlled. The critical parameter in bending is the L/b ratio, where L is the body length of an IC, or the length from lead bend to lead bend on large axial lead parts, and b is the length of the PWB parallel to the part. As this ratio approaches one, the ability of the board to deflect decreases, leaving no stress relief for the parts. Therefore, good PWA design layout practices should avoid large leadless chip carriers (LCCs), ICs, and large axial lead parts centrally located and parallel to the short side of the PWB. The maximum allowable deflection of typical parts can be calculated using the following equations.

5.4.2.1 Maximum Allowable Deflection Of ICs

The maximum allowable PWB deflection (δ_{\max}) for an IC can be calculated using equation 5-6. This value is the largest PWB deflection that the IC can withstand before lead damage or fatigue occurs. This calculation is then used in Section 5.4.2.4 to determine the

maximum allowable input PSD level which for the tested IC. The PSD level is calculated using the smallest expected deflection as determined in Equation 5-3.

$$\delta_{\max} = \left[\frac{(4.19 \times \sigma_{\max} \times l_1^2)}{E \times h} \right] \times \left[\frac{b}{L} \right]^2 \quad \text{Eq. 5-6}$$

where: σ_{\max} = Endurance limit (Se) of the IC lead material, psi.

5.4.2.2 Maximum Allowable Deflection For Axial Lead Parts

When axial lead parts are vibrated in an axis perpendicular to their bodies and the PWB, they tend to react in two major motions (bending and twisting). Bending motion occurs when the part vibrates up and down along a perpendicular axis through the body of the part. When the part is in bending it tends to fatigue at the lead bends and the lead ends. Twisting motion occurs when the part attempts to spin about an imaginary point located on the part body. This motion also causes lead fatigue. The method used to analyze these parts calculates the maximum deflection allowed by the twisting motion and the maximum deflection allowed by the bending motion and uses the smaller of these two values to calculate the maximum allowable PSD input level along with the expected board deflection for equation 5-3 in Section 5.4.2.4. The smaller value will be the limiting factor in the motion of the part. This method then, limits the stress to the highest level obtainable without causing structural damage to the part leads. Equation 5-7 is the formula for the maximum allowable deflection due to twisting motion and Equation 5-8 is the formula for the maximum allowable deflection due to bending motion.

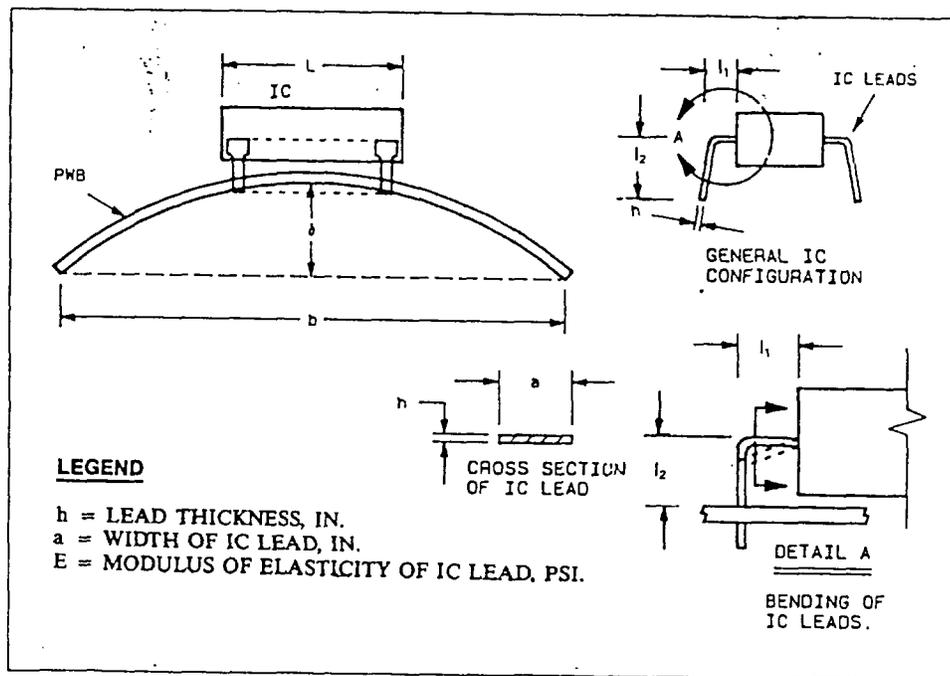


Figure 5-1. Maximum Allowable Deflection for ICs

TWISTING

$$\text{For } l_2 > l_1, \quad \delta_{\max} = \left[\frac{4 \times \sigma_{\max}}{\pi^2 \times E \times d} \right] \times \left[\frac{l_2}{4} \right] \times \left[\frac{b^2}{L} \right] \quad \text{Eq. 5-7a}$$

$$\text{For } l_2 = l_1, \quad \delta_{\max} = \left[\frac{4 \times \sigma_{\max}}{\pi^2 \times E \times d} \right] \times \left[\frac{l_1 + l_2}{4} \right] \times \left[\frac{b^2}{L} \right] \quad \text{Eq. 5-7b}$$

$$\text{For } l_1 > l_2, \quad \delta_{\max} = \left[\frac{4 \times \sigma_{\max}}{\pi^2 \times E \times d} \right] \times [2l_1] \times \left[\frac{b^2}{L} \right] \quad \text{Eq. 5-7c}$$

where: σ_{\max} = Endurance limit (Se) of the axial lead material, psi.
 E = Modulus of elasticity, psi.

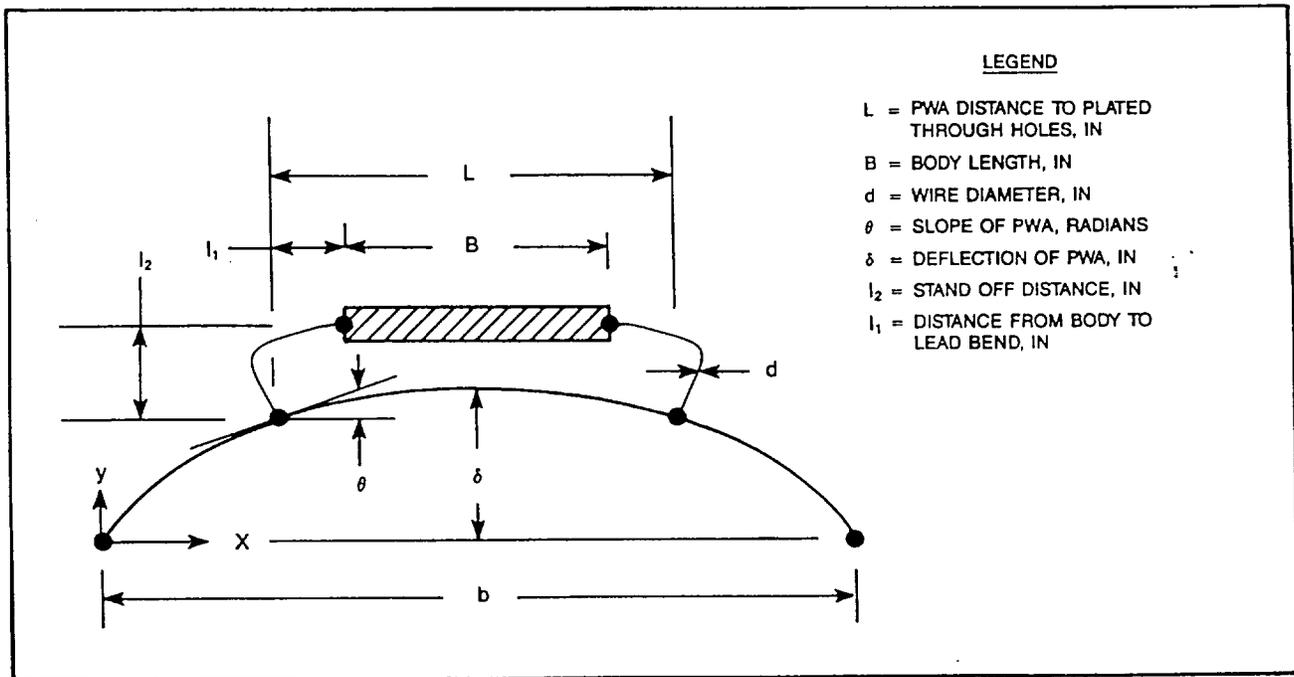


Figure 5-2. Discrete Axial Lead Parts

BENDING

$$\delta_{\max} = \left[\frac{F \times \sigma_{\max} \times l_1^2}{E \times d} \right] \times \left[\frac{b}{L} \right]^2 \quad \text{Eq. 5-8}$$

where: σ_{\max} = Endurance limit (Se) of the axial lead material, psi.
and

$$\text{If } 0.1 < \frac{l_2}{l_1} < 4.0, \quad \text{then } F = 1.048 \times \left(\frac{l_2}{l_1} \right)$$

$$\text{If } \frac{l_2}{l_1} > 4.0, \quad \text{then } F = 4.19$$

$$\text{If } \frac{l_2}{l_1} < 0.1, \quad \text{then } F = 0.1$$

5.4.2.3 Maximum Allowable Deflection For LCCs

When a Leadless Chip Carrier (LCC) is vibrated in an axis perpendicular to its body the solder tends to lift from the fillet land. This is a result of PWB bending stresses. The analysis for the LCC is shown in Equation 5-9 and calculates the maximum allowable deflection that the solder fillets can withstand before they are stressed beyond the solder materials' endurance limits. Once the maximum allowable deflection for the LCC has been calculated, it will be used in Section 5.4.2.4 along with the expected deflection from Equation 5-3 to determine the maximum allowable PSD input level for this part.

$$\delta_{\max} = \left[\frac{\sigma_{\max} \times l_s}{E} \right] \times \left[\frac{b}{L} \right]^2 \quad \text{Eq. 5-9}$$

where: σ_{\max} = Endurance limit (Se) of the solder, psi.
 l_s = Effective length of the solder joint, inches.
E = Modulus of Elasticity of the solder, psi.

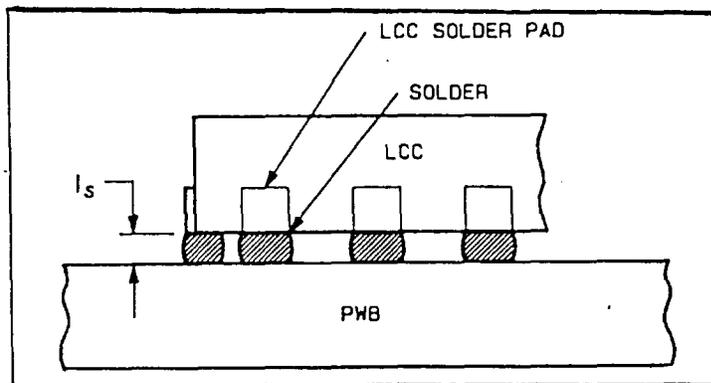


Figure 5-3. LCC Solder Interconnections

5.4.2.4 Maximum Allowable PSD Input Level For A Part Vibrated Perpendicular To Its Body And PWB

If a part is vibrated perpendicular to its body, the maximum allowable PSD input level is calculated using the following steps. First, calculate the expected deflection of the PWB and the expected deflection of the thermal plane and use the smaller of the two values from Equation 5-3. Use the applicable Section (5.4.2.1 through 5.4.2.3) to calculate the maximum allowable deflection. Once these values have been calculated, insert them in Equation 5-10. This determines the maximum allowable PSD level at which this particular part can be vibrated based on its material properties.

$$PSD_{\max} = \left[\frac{\delta_{\max}}{\delta_{ex}} \right]^2 \times .04 \frac{g^2}{Hz} \quad \text{Eq. 5-10}$$

This is the maximum allowable input PSD level for the part being analyzed in the z axis.

5.4.3 MAXIMUM ALLOWABLE PSD LEVEL FOR TOMBSTONE TYPE PARTS VIBRATED IN THE Z AXIS

One part type that is critical in bending is a large tombstone type part. In most cases, they are bent over to lower the center of gravity which reduces some of the stresses associated with their use. This technique is beneficial in some ways but the high center of gravity still tends to cause motion of this part during Z axis vibration. The tombstone type part is bent in the shape shown in Figure 5-4. The center of gravity of these parts is normally high off the PWB and the motion is in a plane perpendicular to the body of the part. If the part body is bonded to the PWB, it does not pose a vibration problem.

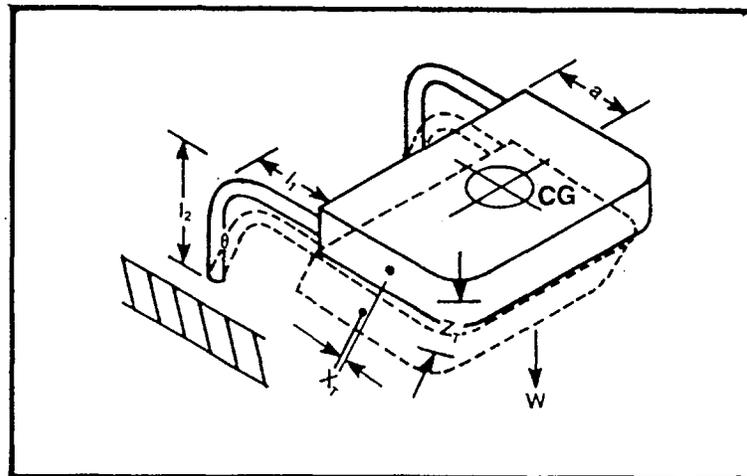


Figure 5-4. Tombstone Type Parts.

The part is not treated like other parts that have forces applied perpendicular to the PWB, because the stresses are not related to PWB bending. The first step in calculating the stresses on these parts is to determine the motion that they will experience.

Due to its odd shape, calculations must determine the position of the part in the X and Z axes during its oscillations. Those values will be designated as X_T and Z_T , (See Equations 5-11 and 5-12 respectively). Because this is not a purely linear motion, a factor for Z_{T2} must be calculated using Equation 5-13. The parameters for these calculations are the weight of the part in pounds (W), the height from the PWB to the lead bend in inches (l_2), the length from the lead bend to the part edge in inches (l_1), the length from the edge of the part to its center of gravity in inches (a), the moment of inertia (I) for the part, and (d) the diameter of the lead.

$$X_T = \left[\frac{W \times (a + l_1) \times l_2^2}{4 \times E \times I} \right] \quad \text{where: } I = 0.049d^4 \quad \text{Eq. 5-11}$$

$$Z_T = \left[\frac{W}{12 \times E \times I} \right] \times [2l_1^3 + 3al_1^2 + 6l_1^2l_2^2 + 6al_1l_2] \quad \text{Eq. 5-12}$$

$$Z_{T2} = (\text{non-linear motion factor}) = Z_T \times \left[\frac{a + l_1}{l_1} \right] \quad \text{Eq. 5-13}$$

The next step in this process is to calculate the deflection of the center of gravity of the part due to a 1G (static) load, as shown in Equation 5-14. This depicts the deflection of the part due to its own weight. The natural frequency of the part can then be calculated using Equation 5-15.

$$\delta_{(1G)} = \sqrt{X_T^2 + Z_{T2}^2} \quad \text{Eq. 5-14}$$

$$f_n = \frac{3.13}{\sqrt{\delta_{(1G)}}} \quad \text{Eq. 5-15}$$

The moment in the lead wires produced by its body weight can now be calculated using Equation 5-16. Using the moment, the stress on the lead wires can be calculated using Equation 5-17.

$$M = \frac{(a + l_1) \times w}{2} \quad \text{Eq. 5-16}$$

$$\sigma_{(1G)} = \frac{M \times \left(\frac{d}{2}\right)}{I} \quad \text{Eq. 5-17}$$

Finding the magnification factor (Q) of the lead wires is the next step. Q is dependent upon the damping ratio (ζ) and is approximately 62.5 for part lead wires. If the damping ratio is known, Equation 5-18 can be used to determine the actual magnification factor.

$$Q = \frac{1}{2\zeta} \quad \text{Eq. 5-18}$$

The G level on the part can now be calculated. Using Crandall's equation and ω_0 equal to .04, G_{out} is calculated as shown by Equation 5-19.

$$G_{out} = \sqrt{\frac{\pi}{2} \times f_n \times Q \times \omega_0} = 1.98 \times \sqrt{f_n} \quad \text{Eq. 5-19}$$

The stress on the lead wire can now be calculated by Equation 5-20.

$$\sigma_{LW} = \sigma_{(1G)} \times G_{out} \quad \text{Eq. 5-20}$$

With the stress level on the lead wires now determined, the maximum allowable G level that this part can withstand (G_{max}) can be calculated using Equation 5-21. The endurance limit of the lead wire material is provided in Appendix B.

$$G_{max} = \frac{6 \sigma_{max}}{\sigma_{LW}} \quad \text{Eq. 5-21}$$

where: σ_{max} = Endurance limit (Se) of the lead material, in psi.

Using the G_{max} value just calculated, the maximum allowable PSD input level can be calculated using Equation 5-22.

$$PSD_{max} = \left[\frac{G_{max}}{6} \right]^2 \times .04 \frac{g^2}{HZ} \quad \text{Eq. 5-22}$$

5.4.4 MAXIMUM ALLOWABLE PSD LEVEL IN LATERAL VIBRATION

The lateral vibration is as critical as perpendicular vibration. The problem is usually with large mass axial lead or metal can type parts. When vibration is applied in a lateral direction, the part's weight will cause it to rock back and forth, which can result in lead wire fatigue. It may be difficult to compensate for lateral vibration if large parts are used.

Therefore, large axial lead parts should be bonded to the PWB. If this cannot be achieved, the following technique shall be followed to determine the maximum allowable PSD input level. There are two different techniques, one for axial lead parts and the other for metal can type parts. Metal clips and wire straps have proven ineffective for holding large axial leaded components unless combined with RTV or other bonding agent.

5.4.4.1 Axial Lead Parts In Lateral Vibration

Lateral motion occurs when an axial lead part is vibrated in a direction perpendicular to its body and parallel with the PWB surface. The parts move back and forth in an arc. This movement tends to fatigue the metal leads at the lead bends and ends. In order to prevent this fatigue, a vibration level must be calculated that will sufficiently vibrate the parts and the leads without causing fatigue damage. In order to accomplish this, the deflection of the part, due to a 1G (static) load, is determined using the parameters in Figure 5-5 and Equation 5-23.

$$\delta_{(1G)} = \left[\frac{W}{6 \times E \times I} \right] \times [l_1^3 + 4l_2^2 l_1 + l_2^3] \quad \text{Eq. 5-23}$$

where: $I = .049d^4$
 $W = \text{weight of the part}$

Using the deflection due to self weight, the natural frequency of the part can be calculated using Equation 5-24.

$$f_n = \frac{3.13}{\sqrt{\delta_{(1G)}}} \quad \text{Eq. 5-24}$$

Next, calculate the bending and shear stresses for the 1G (static) load. The two stresses are calculated such that the overall stress on the lead wires can be determined. The bending stress is calculated by using Equation 5-25 and the shear stress by Equation 5-26.

$$\sigma_A = \frac{W \times l_2 \times d}{4I} \quad \text{Eq. 5-25}$$

$$\tau_A = \frac{W \times l_1 \times d}{8I} \quad \text{Eq. 5-26}$$

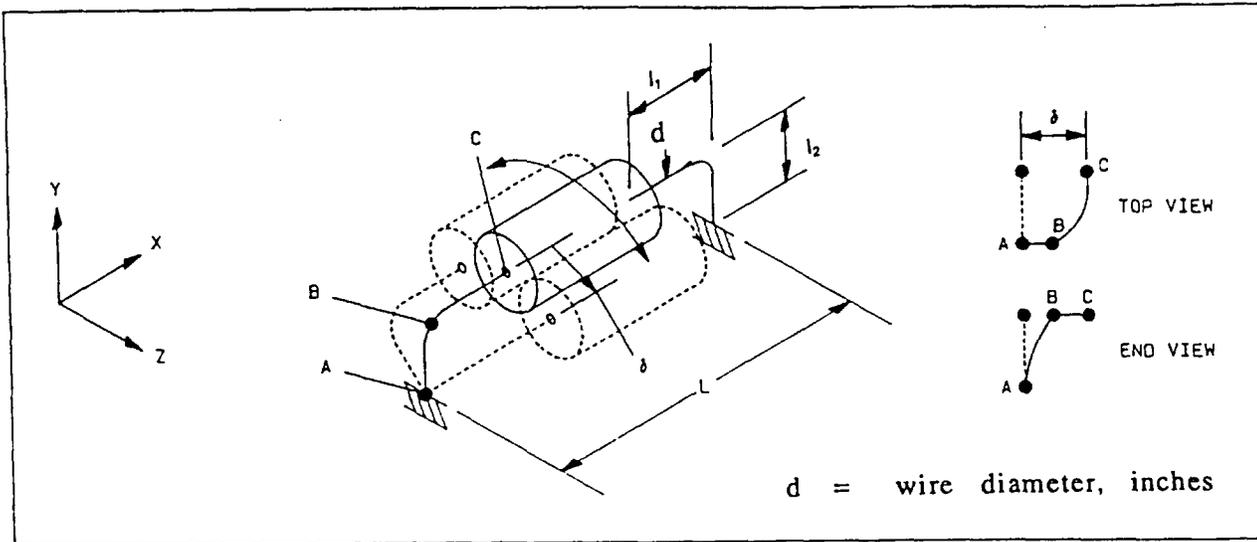


Figure 5-5. Axial Lead Parts

Using the principles of Mohr's circle and the values calculated for bending and shear stresses, the principal stress due to a static load can be calculated using Equation 5-27. Equation 5-28 represents the principal stress accounting for a typical radius of the lead bend.

$$\sigma'_A = \frac{\sigma_A}{2} + \sqrt{\left[\frac{\sigma_A}{2}\right]^2 + \tau_A^2} \quad \text{Eq. 5-27}$$

$$\sigma_{A2} = 2.1 \times \sigma'_A \quad \text{Eq. 5-28}$$

Using Crandall's equation, a value for Q equal to 62.5, and ω_0 equal to .04, the G_{out} level can be calculated as shown in Equation 5-29.

$$G_{out} = \sqrt{\frac{\pi}{2} \times f_n \times Q \times \omega_0} = 1.98 \sqrt{f_n} \quad \text{Eq. 5-29}$$

This G level is used in Equation 5-30 to determine the stress on the lead wires.

$$\sigma_{LW} = G_{out} \times \sigma_{A2} \quad \text{Eq. 5-30}$$

The G_{max} of the part is calculated using the endurance limit of the lead material (σ_{max}) from Appendix B and the calculated stress level on the lead wire as shown in Equation 5-31. The Maximum Allowable PSD level is obtained from Equation 5-32.

$$G_{max} = \frac{6 \sigma_{max}}{\sigma_{LW}} \quad \text{5-31}$$

$$PSD_{max} = \left[\frac{G_{max}}{6} \right]^2 \times .04 \frac{g^2}{Hz} \quad \text{Eq. 5-32}$$

5.4.4.2 Metal Can Type Parts

The another part type to consider in lateral vibration is the metal can type parts, including transistors and small hybrids. They are usually mounted perpendicular to the PWB surface, have no lead bends, and can have any number of leads. The calculation for this part is similar to the lateral vibration for axial lead parts with a few minor changes. The parameters required to perform this calculation are represented in Figure 5-6 and defined as the number of lead wires (n), the length of the lead wire from the part to the PWB in inches (l), the weight of the part in pounds (W), and the length from the edge of the part body to the center of gravity of the part in inches (a). The first step in this procedure is to calculate the deflection of the part due to its self weight using Equation 5-33. Once the deflection is known, the natural frequency of the part can be calculated as shown in Equation 5-34.

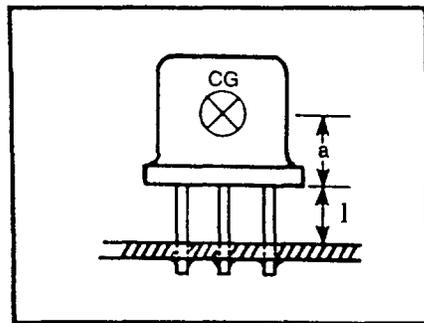


Figure 5-6. Metal Can Type Part

$$\delta_{(1G)} = \left[\frac{W \times l}{n \times E \times I} \right] \times \left[\frac{l^2}{3} + \frac{a \times l}{2} + a^2 \right] \quad \text{Eq. 5-33}$$

$$f_n = \frac{3.13}{\sqrt{\delta_{(1G)}}} \quad \text{Eq. 5-34}$$

The stress applied to the lead wires due to the static load can be calculated using equation 5-35. This is the amount of stress that is applied to the lead wires while it is motionless on the PWB.

$$\sigma_{(1G)} = \frac{W \times l \times \frac{d}{2}}{n \times I} \quad \text{Eq. 5-35}$$

where: $I = .049d^4$

Using the natural frequency calculated for a static load, a value for Q equal to 62.5, and the PSD level (ω_0) equal to 0.04, the G_{out} level can be determined using the Crandall equation shown as Equation 5-36.

$$G_{out} = \sqrt{\frac{\pi}{2} \times f_n \times Q \times \omega_0} = 1.98 \times \sqrt{f_n} \quad \text{Eq. 5-36}$$

The stress on the lead wires due to vibration is calculated by multiplying the stress for static loading by the G_{out} level as shown in Equation 5-37.

$$\sigma_{LW} = G_{out} \times \sigma_{(1G)} \quad \text{Eq. 5-37}$$

The maximum allowable G level for this part can then be determined by using the endurance limit of the lead wire material from Appendix B and the stress applied to the lead wires using Equation 5-38. The maximum allowable PSD level is determined as shown in Equation 5-39.

$$G_{max} = \frac{6 \sigma_{max}}{\sigma_{LW}} \quad \text{5-38}$$

$$PSD_{max} = \left[\frac{G_{max}}{6} \right]^2 \times .04 \frac{g^2}{HZ} \quad \text{Eq. 5-39}$$

5.5 ASSEMBLIES TO BE CONSIDERED FOR VIBRATION SCREENING DELETION

There are several types of hardware that will not benefit from a vibration screen and may even be degraded from an improperly applied vibration screen. Some of the items that should be considered for deletion of vibration screening are listed below. In many cases, the vibration screen may be deleted on these assemblies if an effective thermal screen can be performed.

5.5.1 WIRE WRAPPED BACKPLANES

Wire wrapped backplanes (WWB) often receive a vibration screen at the NAVMAT levels. These screens generally prove ineffective at finding workmanship defects but are helpful in "cleaning up" debris that is left from the manufacturing of the backplanes. If the WWB's need to be cleaned, a .01 g²/Hz random vibration can be performed that will remove the debris. This vibration should not be considered as part of the screening process, but as a manufacturing process. WWBs and backplanes should only be screened if they contain parts or workmanship that may benefit from a properly developed screening process.

5.5.2 MECHANICAL HARDWARE

Purely mechanical hardware should not receive screening. Purely mechanical hardware is defined as hardware that contains only mechanical parts. Other systems that can be included in this category are mechanical systems that contain very limited electrical hardware, e.g. antennas, fuse boxes, and switch boxes. These units will not benefit from screening and should not be screened. Mechanical devices will generally have a reduced life if they are subjected to screening. The reduction in life is small but the screen will not surface any defects that will justify screening.

5.5.3 DISPLAYS

Electronic displays, e.g. Liquid Crystal Displays (LCD) and vacuum displays, should not be screened by either random vibration or thermal cycling. Displays that are subjected to screen will experience degradation and/or hard failures. Thermal cycling will create stress fractures in the glass materials due to the differences in thermal coefficients of expansions and vibration will crack the displays.

APPENDIX A

*PRINTED WIRING BOARD
NATURAL FREQUENCY EQUATIONS*

APPENDIX A

PRINTED WIRING BOARD NATURAL FREQUENCY EQUATIONS

The following is a list of PWB conditions with their respective natural frequency equation. The first series of equations are for rectangular PWBs with varying edge conditions, and the second series of equations for odd shaped PWB configurations. These equations, when evaluated, will provide the user an approximation of the natural frequency (f_n).

The parameters for these equations are as follows:

where: E = modulus of elasticity of PWB
t = thickness of the PWB
 μ = poisson's ratio of the PWB; if unknown, use a value of 0.3
D = stiffness factor of the PWB
 ρ = mass per unit area of the
W = weight of the PWA
area = area of PWB material equal to a times b for rectangle
a = long side of the PWB
b = short side of the PWB
g = force of gravity: 32.2 ft/sec² or 386 in/sec²

$$d = \frac{E \times t^3}{12 (1 - \mu^2)}$$

$$\rho = \frac{w}{\text{area} \times g}$$

- NOTES: 1) The above equations apply to thermal planes as well as PWAS.
2) For odd-shaped PWAS, use the plate that best fits the actual PWA.

Key:

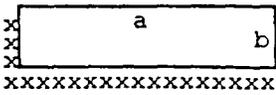
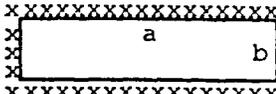
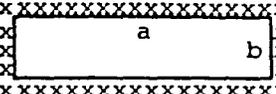
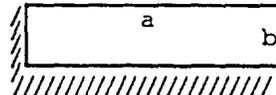
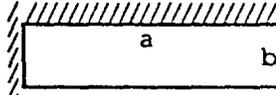
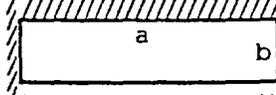
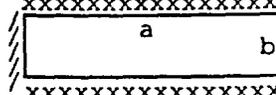
Free Edge

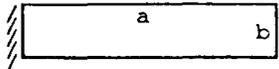
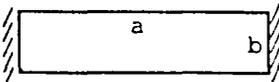
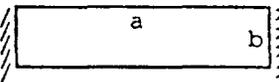
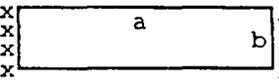
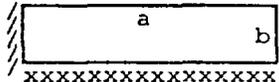
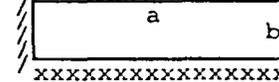
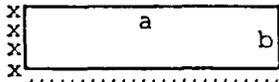
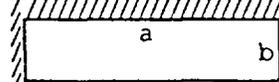
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Supported Edge

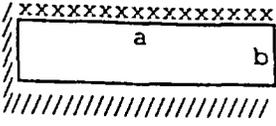
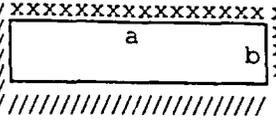
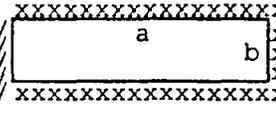
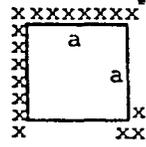
//////
Fixed Edge

Equation

Plate

$f_n = \frac{\pi}{8} \left(\frac{D}{\rho} \right)^{1/2} \left(\frac{1}{a^2} + \frac{1}{b^2} \right)$	
$f_n = \frac{\pi}{2} \left(\frac{D}{\rho} \right)^{1/2} \left(\frac{1}{4a^2} + \frac{1}{b^2} \right)$	
$f_n = \frac{\pi}{2} \left(\frac{D}{\rho} \right)^{1/2} \left(\frac{1}{a^2} + \frac{1}{b^2} \right)$	
$f_n = \frac{\pi}{5.42} \left[\frac{D}{\rho} \left(\frac{1}{a^4} + \frac{3.2}{a^2b^2} + \frac{1}{b^4} \right) \right]^{1/2}$	
$f_n = \frac{\pi}{3} \left[\frac{D}{\rho} \left(\frac{0.75}{a^4} + \frac{2}{a^2b^2} + \frac{12}{b^4} \right) \right]^{1/2}$	
$f_n = \frac{\pi}{1.5} \left[\frac{D}{\rho} \left(\frac{3}{a^4} + \frac{2}{a^2b^2} + \frac{3}{b^4} \right) \right]^{1/2}$	
$f_n = \frac{\pi}{3.46} \left[\frac{D}{\rho} \left(\frac{16}{a^4} + \frac{8}{a^2b^2} + \frac{3}{b^4} \right) \right]^{1/2}$	

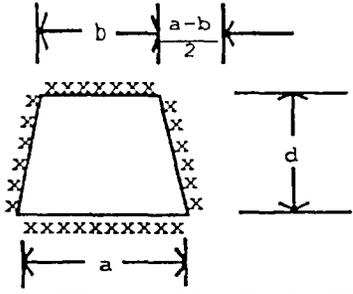
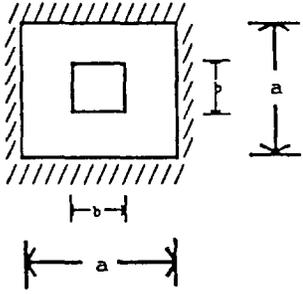
$f_n = \frac{0.56}{a^2} \left(\frac{D}{\rho} \right)^{1/2}$	
$f_n = \frac{3.55}{a^2} \left(\frac{D}{\rho} \right)^{1/2}$	
$f_n = \frac{0.78\pi}{a^2} \left(\frac{D}{\rho} \right)^{1/2}$	
$f_n = \frac{\pi}{2a^2} \left(\frac{D}{\rho} \right)^{1/2}$	
$f_n = \frac{\pi}{1.74} \left[\frac{D}{\rho} \left(\frac{4}{a^4} + \frac{1}{2a^2b^2} + \frac{1}{64b^4} \right) \right]^{1/2}$	
$f_n = \frac{\pi}{2} \left[\frac{D}{\rho} \left(\frac{0.127}{a^4} + \frac{0.20}{a^2b^2} \right) \right]^{1/2}$	
$f_n = \frac{\pi}{2} \left[\frac{D}{\rho} \left(\frac{1}{a^4} + \frac{0.608}{a^2b^2} + \frac{0.126}{b^4} \right) \right]^{1/2}$	
$f_n = \frac{\pi}{2} \left[\frac{D}{\rho} \left(\frac{2.45}{a^4} + \frac{2.90}{a^2b^2} + \frac{5.13}{b^4} \right) \right]^{1/2}$	

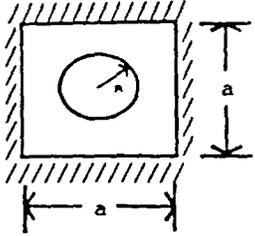
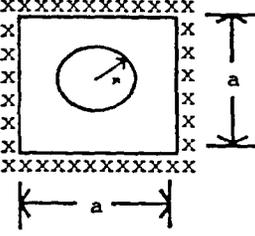
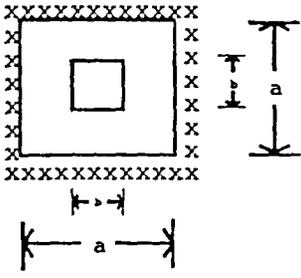
$f_n = \frac{\pi}{2} \left[\frac{D}{\rho} \left(\frac{0.127}{a^4} + \frac{0.707}{a^2b^2} + \frac{2.44}{b^4} \right) \right]^{1/2}$	
$f_n = \frac{\pi}{2} \left[\frac{D}{\rho} \left(\frac{2.45}{a^4} + \frac{2.68}{a^2b^2} + \frac{2.45}{b^4} \right) \right]^{1/2}$	
$f_n = \frac{\pi}{2} \left[\frac{D}{\rho} \left(\frac{2.45}{a^4} + \frac{2.32}{a^2b^2} + \frac{1}{b^4} \right) \right]^{1/2}$	
$f_n = \frac{4.50}{\pi a^2} \left(\frac{D}{\rho} \right)^{1/2}$	

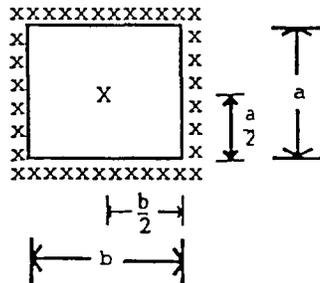
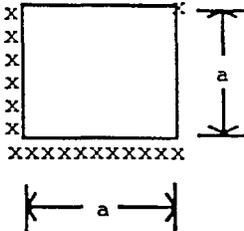
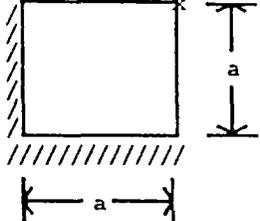
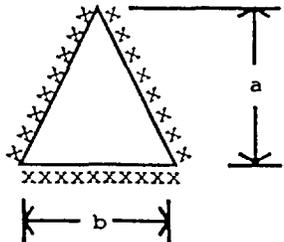
ODD SHAPE PWB CONDITIONS

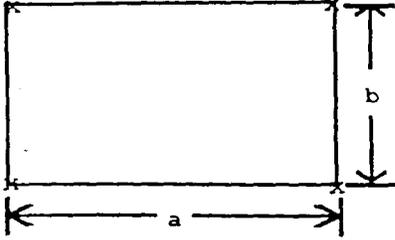
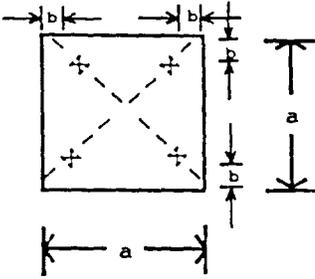
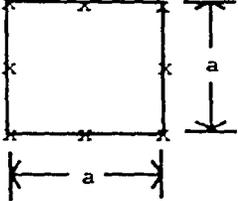
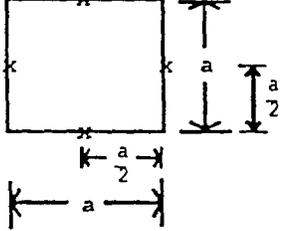
Notation t = thickness of plate;
 E = modulus of elasticity;
 ρ = mass per unit area of plate (dt for a plate of material with density d);
 μ = Poisson's ratio

Fundamental Natural Frequency (hertz), $f_n = \frac{\lambda^2}{2\pi a^2} \left[\frac{Et^3}{12\rho(1-\mu^2)} \right]^{1/2}$

Description	λ^2																																										
<p>Simply Supported Symmetric Trapezoid</p> 	<table border="1" data-bbox="727 898 1367 1033"> <thead> <tr> <th>$\frac{d}{a}$</th> <th colspan="6">b/a</th> </tr> <tr> <th></th> <th>0.0</th> <th>0.2</th> <th>0.4</th> <th>0.6</th> <th>0.8</th> <th>1.0</th> </tr> </thead> <tbody> <tr> <td>0.5</td> <td>98.78</td> <td>76.50</td> <td>63.18</td> <td>55.97</td> <td>51.85</td> <td>49.35</td> </tr> <tr> <td>2/3</td> <td>69.70</td> <td>55.09</td> <td>44.70</td> <td>38.38</td> <td>34.54</td> <td>32.08</td> </tr> <tr> <td>1.0</td> <td>45.85</td> <td>37.75</td> <td>30.79</td> <td>25.64</td> <td>22.13</td> <td>19.74</td> </tr> <tr> <td>1.5</td> <td>32.74</td> <td>28.04</td> <td>23.64</td> <td>19.72</td> <td>16.58</td> <td>14.26</td> </tr> </tbody> </table>	$\frac{d}{a}$	b/a							0.0	0.2	0.4	0.6	0.8	1.0	0.5	98.78	76.50	63.18	55.97	51.85	49.35	2/3	69.70	55.09	44.70	38.38	34.54	32.08	1.0	45.85	37.75	30.79	25.64	22.13	19.74	1.5	32.74	28.04	23.64	19.72	16.58	14.26
$\frac{d}{a}$	b/a																																										
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1.5	32.74	28.04	23.64	19.72	16.58	14.26																																					
<p>Fixed Plate, Square Opening</p> 	<table data-bbox="706 1297 1383 1438"> <tbody> <tr> <td>$\frac{b}{a}$</td> <td>= 0</td> <td>1/16</td> <td>1/3</td> <td>1/2</td> </tr> <tr> <td>λ^2</td> <td>= 34.85</td> <td>35.80</td> <td>43.25</td> <td>62.43</td> </tr> </tbody> </table>	$\frac{b}{a}$	= 0	1/16	1/3	1/2	λ^2	= 34.85	35.80	43.25	62.43																																
$\frac{b}{a}$	= 0	1/16	1/3	1/2																																							
λ^2	= 34.85	35.80	43.25	62.43																																							

Description	λ^2
<p>Fixed Plate, Circular Opening</p> 	$\frac{2R}{a} = 0.0 \quad 0.05 \quad 0.10 \quad 0.15 \quad 0.20 \quad 0.25$ $\lambda^2 = 36.0 \quad 35.5 \quad 35.1 \quad 35.2 \quad 35.7 \quad 36.3$
<p>Simply Supported Plate, Round Opening</p> 	$\frac{2R}{a} = 0 \quad 0.05 \quad 0.10 \quad 0.15 \quad 0.20 \quad 0.25 \quad 0.3$ $\lambda^2 = 19.9 \quad 19.75 \quad 19.5 \quad 19.4 \quad 19.3 \quad 19.35 \quad 19.5$
<p>Simply Supported Plate, Square Opening</p> 	$\frac{b}{a} = 0 \quad 1/6 \quad 1/3 \quad 1/2$ $\lambda^2 = 19.63 \quad 19.48 \quad 21.45 \quad 26.05$

Description	λ^2												
<p>Rectangular Plate with Simply Supported Edges with a Center Pinned Support</p> 	<table border="0"> <tr> <td>$\frac{a}{b}$</td> <td>=</td> <td>1.0</td> <td>1.5</td> <td>2.0</td> </tr> <tr> <td>λ^2</td> <td>=</td> <td>52.6</td> <td>73.1</td> <td>91.1</td> </tr> </table>	$\frac{a}{b}$	=	1.0	1.5	2.0	λ^2	=	52.6	73.1	91.1		
$\frac{a}{b}$	=	1.0	1.5	2.0									
λ^2	=	52.6	73.1	91.1									
<p>Square Plate with Two Simply Supported Sides and a Pinned Support at Corner</p> 	<p>$\lambda^2 = 9.00$</p>												
<p>Square Plate with Two Fixed Sides and a Pinned Support at Center</p> 	<p>$\lambda^2 = 13.7$</p>												
<p>Simply Supported Isosceles Triangle</p> 	<table border="0"> <tr> <td>$\frac{a}{b}$</td> <td>=</td> <td>0.5</td> <td>2/3</td> <td>1.0</td> <td>1.5</td> </tr> <tr> <td>λ^2</td> <td>=</td> <td>24.69</td> <td>30.98</td> <td>45.85</td> <td>73.66</td> </tr> </table>	$\frac{a}{b}$	=	0.5	2/3	1.0	1.5	λ^2	=	24.69	30.98	45.85	73.66
$\frac{a}{b}$	=	0.5	2/3	1.0	1.5								
λ^2	=	24.69	30.98	45.85	73.66								

Description	λ^2
<p>Rectangular Plate, Pinned Corner Supports</p> 	$\frac{a}{b} = 1.0 \quad 1.5 \quad 2.0 \quad 2.5$ $\lambda^2 = 7.12 \quad 8.92 \quad 9.29 \quad 9.39$
<p>Square Plate, Four Point Supports</p> 	$\frac{b}{a} = 0.0 \quad 0.1 \quad 0.2 \quad 0.3 \quad 0.4 \quad 0.5$ $\lambda^2 = 7.14 \quad 12.89 \quad 19.69 \quad 19.31 \quad 13.35 \quad 11.34$
<p>Square Plate, with n Equally Spaced Point Supports on Edges</p>  <p>($n = 3$ shown)</p>	$n = 3 \quad 5 \quad 7 \quad 9 \quad \infty^*$ $\lambda^2 = 18.20 \quad 19.64 \quad 19.71 \quad 19.73 \quad 19.74$ $\infty^* = \text{Simply Supported Edges}$
<p>Square Plate, Pinned Supports at Midpoints of Sides</p> 	$\lambda^2 = 13.5$

APPENDIX B

*ENDURANCE LIMITS (S_e) AND MODULUS
OF ELASTICITY (E) FOR VARIOUS
MATERIALS*

Material	Sc (est) psi	E (est) psi
G-10	20,000	2.00 X 10 ⁶
Polymide	18,000	2.75 X 10 ⁶
Aluminum Oxide	12,500	45.0 X 10 ⁶

TABLE B-1. PWB AND THERMAL PLAN MATERIAL PROPERTIES

Lead Material*	SE (est) psi	E (est) psi
Kovar	38,750	20 X 10 ⁶
Alloy 42	35,000	21 X 10 ⁶
Steel	33,000	30 X 10 ⁶
Nickel	28,000	31 X 10 ⁶
Copper (hard)	17,000	17 X 10 ⁶
Copper (soft)	11,000	17 X 10 ⁶

TABLE B-2. LEAD MATERIAL PROPERTIES

*NOTE: If parts are being procured to a Qualified Products List where more than one type of lead material is possible, the lowest endurance limit must be used.

Sn/Pb/In Sn = % tin Pb = % lead In = % indium	Se (est) psi	E (est) psi
63/37/-	3100	4.6 X 10 ⁶
50/-/50	690	3.4 X 10 ⁶
50/50/-	2500	18. X 10 ⁶
-/50/50	1870	2.0 X 10 ⁶

TABLE B-3. SOLDER MATERIAL PROPERTIES

REFERENCES

1. Crandell, Steven H., "Random Vibration in Mechanical Systems", New York: Academic Press, 1963.
2. Institute of Environmental Sciences, "Environmental Stress Screening Guidelines for Parts", Environmental Stress Screening of Electronic Hardware, September 1985.

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(714) 273-4618
